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МЕТОД УВЕЛИЧЕНИЯ СКОРОСТИ АВТОМАТИЗИРОВАННОГО ВЫРАВНИВАНИЯ ЗАПИСИ СИНХРОННО-ДИНАМИЧЕСКОЙ ПАМЯТИ С ПРОИЗВОЛЬНЫМ ДОСТУПОМ

Рассмотрена процедура выравнивания записи, имеющая ключевую роль в синхронно-динамической памяти с произвольным доступом (СДППД). Цмоделированы и измерены важнейшиие параметры в процедуре, в результате чего выявлено, что при достижении результата поцедура имеет большую задержку. Для увеличения скорости предлагается изменение алгоритмы процедуры.

Ключевые слова: СДППД, синхросигнал, настройка записи, полетная топология.

Z.M. AVETISYAN

A SPEED INCREASING METHOD IN AUTOMATED WRITE LEVELING OF SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY

The procedure of write leveling which has a key role in the synchronous dynamic random access memory (SDRAM) is investigated. The mentioned procedure was modeled and some key parameters were measured. During the investigation, it was found that the procedure has a long delay. For the speed increase, some change is proposed in the write leveling algorithm.

Keywords: SDRAM, clock signal, write leveling, fly-by topology.

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READ AND WRITE CYCLE SPEEDUP METHOD FOR PSEUDO TWO-PORT SRAM WITH A 6T BIT CELL

Two-port 6T SRAM with improved read/write path is presented. The conventional two-port SRAM (2P-SRAM) with an 8T bit cell deliver has the best speed performance, but on the other hand, in some cases, speed can be degraded. To overcome the speed issue and improve the area, a two-port 6T SRAM is proposed, which can speed up the write/read cycle time by 60% and reduce the area by 14%. The disadvantage of this method is the output delay increase.

Keywords: SRAM: performance; speed: decoder; word line; two-port.

Introduction: Nowadays, high-speed SRAM is broadly used in many areas and intended for the cache memory of server systems and networking or mobile

applications**.** SRAM as a random access memory is the fastest memory for write or read operations. High-speed SRAM can immediately access data as soon as enabled read or write is operated at the address. It can read or write data of the address in one cycle of the clock. To speedup High-speed SRAM, we need to reduce the clock cycle time and increase the clock latency. So, one of the main challenges for those devices is the write cycle time. One of the methods for the write cycle time reduction is the bit cell switch, which affects design architecture. It decreases area, but makes the design more complicated. The conventional two-port SRAM is designed with an 8T SRAM bit cell [1], which has the best speed performance compared to other schemes. Moreover, the disadvantage of this method is the area loss, because the 8T bit cell is around 1.5 times larger than the 6T bit cell [2], which results in area increase around 2 times for same memory instance. To overcome all the issues, the pseudo two-port SRAM scheme is proposed.

Problems and justification of the method:

A. Conventional 2P-SRAM with an 8T bit cell

In conventional two-port SRAM with an 8T bit cell, one port is for read, one for write, within one clock cycle. So, from the control block perspective, only one decoder is enough, which will control the word-line selection. Because of separated design of the 8T bit cell with pairs of write bit/word-lines and single ended read bit/word-line [3], it delivers fast access time (Fig. 1).

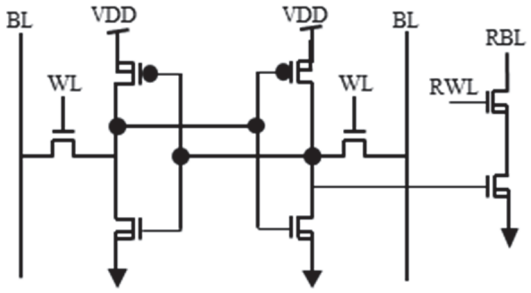

Fig. 1. 8T bit cell with single ended read path

The memory macro area based on the 8T bit cell is 1.5~2x larger than the 6T memory macro, mainly because of a bigger size of the 8T bit cell and additional circuitry of distinguished control and data signals, also during the same row access, the speed will be decreased. However, the function speed cannot be optimized based on the clock-driven design.

B. The proposed pseudo 2P-SRAM with a 6T bit cell

To speed up the read/write path, the split method of control block decoders is proposed (Fig. 2). Instead of 1 decoder it is proposed to use 2 decoders one for read one for write, with cross connected enable signals. The WREN signal disables the decoder intended for the read operation and vice versa, RDEN for the write decoder, other input pins are for read/write data clock signals. Inside the decoders is the same structure irrespective of read or write. In the write decoder with RDEN high signal, the word-line will be disabled and tied to the ground, so the memory row with the bit cell array would not be selected, when RDEN is low, the data from WRCLK will flow through the inverter to output WL (Fig. 3). The output of the cross-connected decoders is the word-line which will activate the appropriate row, consisting of 6T bit cells (Fig. 4). For simplicity, the memory array row with 6T bit cells is presented. They all will be activated when the WL signal is high (Fig. 5).

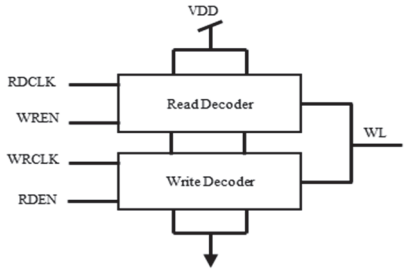

Fig. 2. The structure of the split Read/Write decoders

This will open the pair of the NMOS transistors and the data on the bit-line, and the bit-line inverse will be stored in the cell.

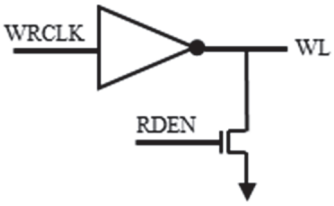

Fig. 3. The contents of the Read/Write decoders

Other than this change in pseudo 2P-SRAM design, the write/read generator scheme is also proposed. This scheme will transfer information from read or write addresses, to WRCLK or RDCLK and drive the decoders.

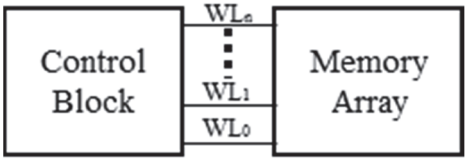

Fig. 4. Structure of selection

In the generator circuit, CLK always toggles as RDADR/WRADR is asserted, which are responsible for the physical address selection of the bit cell, and WRCLK/RDCLK is generated according to the address value (Fig. 6).

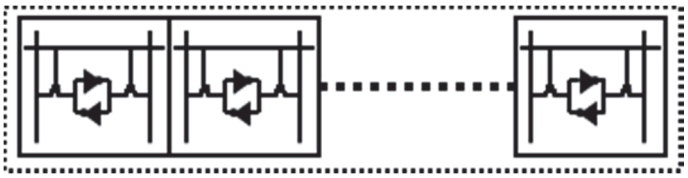

Fig. 5. The memory array row

This method is area and speed efficient for the memory instance with large capacity. Simulation results provided in the next section for 2P-SRAM shows that the function can be 60% faster than the conventional 2P-SRAM design with an 8T bit cell.

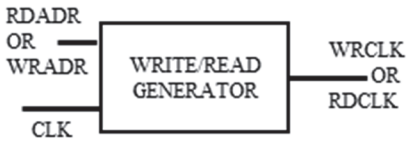

Fig. 6. The write/read generator structure

MEASUREMENT RESULTS: 2560-b 2P-SRAM with a 6T bit cell techniques has been designed in a 28-nm CMOS technology. The memory array is created with 16 physical rows and 160 physical columns. The proposed schemes are implemented in the array control block and in the global center block of the memory instance. The simulation has been performed on 2P-SRAM with conventional and proposed methods for SS (slow-slow) PVT corner with supply voltage and temperature variations using 28nm technology node under 1100MHz and 0.71V VDD voltage level, which corresponds to the SRAM standard. The comparison of the cycle time between the conventional and proposed methods is presented in Table 1.

Table 1

The cycle time and area comparison results for 2P- SRAM

2P-SRAM	Conventional	Proposed	difference (%)
Cycle Time (ps)	954	596	60%
Area (μm^2)	1886.79	1646.65	14%

The only disadvantage of this implementation is time to output data, which is slightly increased, by around 5% (Table 2).

Table 2

The time to output comparison results for 2P-SRAM

2P-SRAM	Conventional	Proposed	difference (%)
Time to output (ps)	436	458	5%

As a result, by applying the proposed schemes in the 2P-SRAM memory, the difference in the cycle time is decreased around 60% and the area around 14%, but at the same time, the time to output is increased by 5%.

CONCLUSION: 2P-SRAM with a 6T bit cell array has been presented with an inbuilt split decoders and read/write generator schemes to speed up the cycle time and decrease the memory instance area of SRAM. This technique saves the memory area and speedup read/write operations. The schemes can be implemented on any 2P-SRAM's. It selectively activates the RDCLK and WRCLK with RDEN and WREN signals and gives an opportunity to decrease the access time. As a result, during the read/write cycles, the cycle time is saved around 60%, and the area is shrunk by 14%. The disadvantage of this method is time to output increase by 5%.

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Ա.Վ. ԱՎԵՏԻՍՅԱՆ

ԸՆԹԵՐՑՄԱՆ ԵՎ ԳՐԱՆՑՄԱՆ ԱՐԱԳԱՈՒԹՅԱՆ ԲԱՐՁՐԱՑՄԱՆ ՄԵԹՈԴ ՊՍԵՎԴՈ ԵՐԿՄԱՏՈՒՅՑ 6S ՍՏԱՏԻԿ ԿԱՄԱՅԱԿԱՆ ԸՆՏՐՈՒԹՅԱՄԲ ՀԻՇԱՍԱՐՔԻ ՀԱՄԱՐ

Ներկայացված է պսևդո երկմատույց ստատիկ կամայական ընտրությամբ հիշասարք (ՍԿԸՀ)՝ բարելավված գրելու/կարդալու ուղիով: Սովորական երկմատույց ստատիկ կամայական ընտրությամբ հիշասարքերը 8S տարրական բջջով ապահովում են լավագույն արագագործությունը, բայց, մյուս կողմից՝ նույն պայմանների դեպքում արագագործությունը կարող է նվազել: Այս խնդիրը հաղթահարելու նպատակով առաջարկվել է 6S տարրական բջջով պսևդո երկմատույց՝ ՍԿԸՀ, որն ունակ է բարձրացնելու ՍԿԸՀ-ի արագագործությունը 60%-ով և նվազեցնելու ՍԿԸՀ-ի զբաղեցրած մակերեսը 14%-ով: Այս մեթոդի թերությունը ելքային տվյալների գրանցման ժամանակի աճն է:

Առանցքային բառեր. ՍԿԸՀ, արդյունավետություն, արագություն, դեկոդեր, բառի գիծ, երկմատույց:

А.В. АВЕТИСЯН

МЕТОД УСКОРЕНИЯ ЦИКЛА ЧТЕНИЯ И ЗАПИСИ ДЛЯ ПСЕВДОДВУХПОРТОВОЙ СТАТИЧЕСКОЙ ПАМЯТИ С ПРОИЗВОЛЬНЫМ ДОСТУПОМ С 6Т ЯЧЕЙКОЙ

Представлена двухпортовая статическая память с произвольным доступом (СППД) с 6Т ячейкой памяти и с улучшенным трактом чтения и записи. Обычная двухпортовая СППД с 8Т ячейкой памяти обеспечивает лучшую скорость работы, но с другой стороны - для некоторых случаев скорость может быть снижена. Предлагается СППД с 6Т ячейкой памяти для преодоления проблемы скорости и улучшения занимаемой площади, которая может ускорить время записи и чтения на 60% и уменьшить площадь на 14%. Недостатком этого метода является увеличение времени выпуска данных.

Ключевые слова: СППД, производительность, скорость, декодер, строка слов, двухпортовый.