UDC 621.3.049

V.A. SAHAKYAN, R.M. SOGHOMONYAN

HIGH PRECISION, VOLTAGE AND TEMPERATURE COMPENSATED CURRENT SOURCE WITH DIGITAL POSTCORRECTION FOR PROCESS VARIATIONS

This paper examines a new technique to reduce the impact of power supply rejection ratio deficiencies in voltage regulators on the performance of current sources that are supplied by these regulators. A voltage regulator with a PMOS output transistor was designed to support 2-mA active load. The technique is relevant for modern 5nm and below technology nodes. SPICE analysis performed over the designed circuit proved the worst case PSRR value as of -35 dB at lower frequencies at wide temperature ranges of -40..125 ° C and supply voltages up to 0.994 V considering the process deviation within ± 4.5 Sigma. Voltage overshoot protection circuit was also developed to ensure safe operation of core devices in various operation modes.

Keywords: voltage regulator, noise, copy, bias voltage.

Introduction. Power supply rejection ratio(PSRR) is a critical parameter that quantifies a regulator's ability to maintain a stable output voltage in the presence of variations in the input supply. Insufficient PSRR can lead to significant output voltage fluctuations, which directly affect the stability and accuracy of current sources. This instability can result in variations in output current, compromising the performance of applications that require precise current regulation. Additionally, the susceptibility of the current source to noise increases, potentially leading to further degradation of system performance. The paper discusses the implications of these PSRR issues, including their effects on thermal performance and reliability, and emphasizes the importance of selecting voltage regulators with adequate PSRR characteristics to ensure optimal current source operation. Recommendations for design considerations and potential mitigation strategies are also provided to enhance the overall performance of systems reliant on VREGs and current sources. Currently, in the process of designing an IC, the on-chip voltage regulators are typically used as an effective method of reducing the impact of noise on supply power delivery networks (PDN). This method reduces the impact of noise and regulates the supply locally, since the location very close to the load needs to have lowest resistance between the supply and the active load. At the same time, such approach reduces the cost of the project and the physical size of the equipment, since there is no need to design additional voltage regulators on the printed circuit board (PCB) and additional input nodes to deliver power, as well as to design the supply network with high-quality and multi-level metal strips. A

typical voltage regulating circuit is an operational amplifier (OPAMP) with negative feedback, the input of which is biased with the required base voltage, and the output is a noise-free supply voltage [1, 2]. As a result of the large input resistance of the OPAMP, the input current is almost zero, which ensures the equality OPAMPs inputs which, in turn, necessitates a fixed output voltage. The capacitor placed at the output of the regulator reduces ripple in the output voltage [1]. The presence of an input LPF ensures the presence of a noise-free voltage at the positive input of the OP AMP. The LPF, which is set to filter the noisy low-level power voltage supplied to the input of the circuit, should ensure as low a cutoff frequency as possible so that incoming low-frequency noise does not get to the output of the circuit. The main reason for these noises is that this voltage is given also to digital IC nodes, in which the switching frequencies in modern circuits are in the GHz range. In order to save IC surface area, the typical cutoff frequency of the input filter is set to 100÷150 kHz range. The elements R and C are selected in such a way that the resistance R is not so large as to cause the transition of the positive input OPAMP to a high resistance state. For this reason, this resistance is selected in the range of 300÷400 kOhm, and a 2.7÷3.5PF capacitor is put in accordance with it [3]. Depending on the type of the output transistor, the voltage regulators are divided into two variants: voltage regulators with P-MOS and N-MOS output transistors [4, 5]. The voltage regulators of N-MOS type are in great demand, however, this type of stabilizer requires the use of auxiliary circuits such as an internal oscillator, voltage multipliers, clock path design, etc. However, unlike the N-MOS voltage stabilizer, the P-MOS type voltage stabilizers do not require auxiliary circuits, but getting a good power supply rejection ratio (PSRR) is quite problematic.

Statement of the Problem. The power supply rejection ratio (PSRR) deficiencies of the voltage regulator (VREG) adversely affect the performance of the current source that derives its supply from the VREG (Fig.1). Insufficient PSRR can lead to output voltage fluctuations at the VREG, which in turn can cause variations in the output current of the current source. This instability may result in degraded performance in applications requiring precise current regulation, increased susceptibility to noise, and potential thermal issues due to inconsistent power delivery.

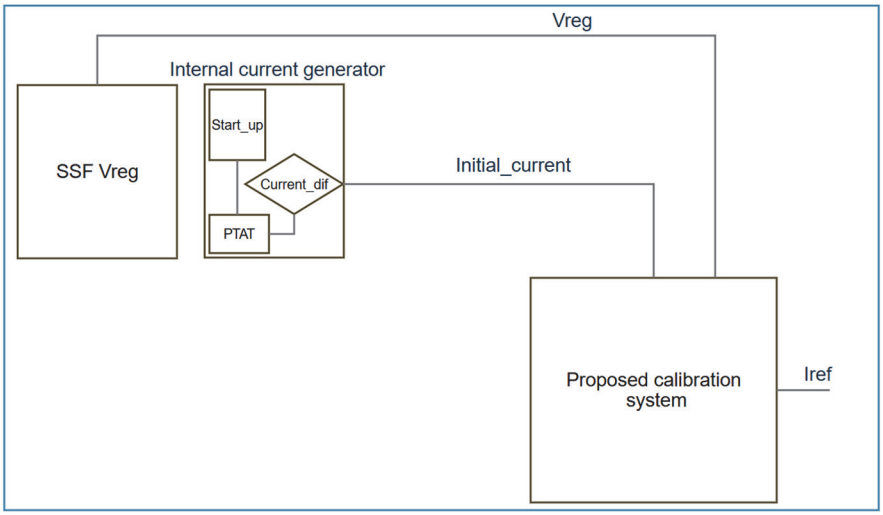

Fig. 1. The block diagram of a high precision current source

The constant increase in IC performance, as well as the application of these circuits in a wide variety of fields, from portable devices to unmanned vehicles, from military equipment to aircraft and spacecraft, force us to take into account the size of IC, power consumption and problems of increasing stability. On the other hand, it is known that the smooth operation of ICs is primarily due to the stability of the current and voltage sources available in them. Hence, it becomes reasonable to develop new methods and solutions that would enhance the effectiveness of the existing measures. The block diagram of the voltage regulator consists of the following main blocks: bias block, slow amp and a fast loop (Fig. 2) [4-6].

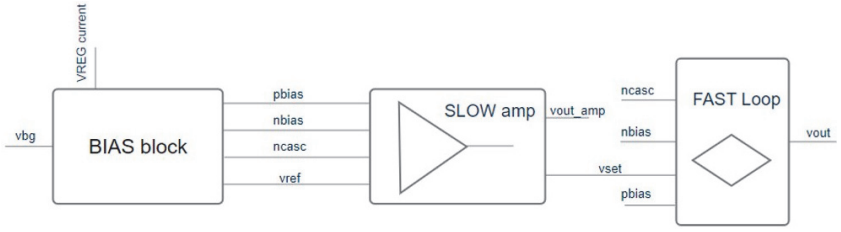

Fig. 2. The block diagram of a PMOS voltage regulator

The Bias block is designed to generate the bias voltage, the Slow amp is designed to determine the operating points of the voltage regulator, and the fast loop - to ensure high system performance.

In standard SSF VREG structures, there is a noise penetration path due to the small resistance r0 of the transistor P1 (Fig. 3). The operational amplifier in the Slow amp reacts to penetrating noise within its speed (loop_1), forming an error

signal at the output of the operational amplifier in order to maintain a constant output signal, but this error signal *vset* enters the output of the voltage regulator without any obstacles because in the fast loop *vset* represents the input of the source follower.

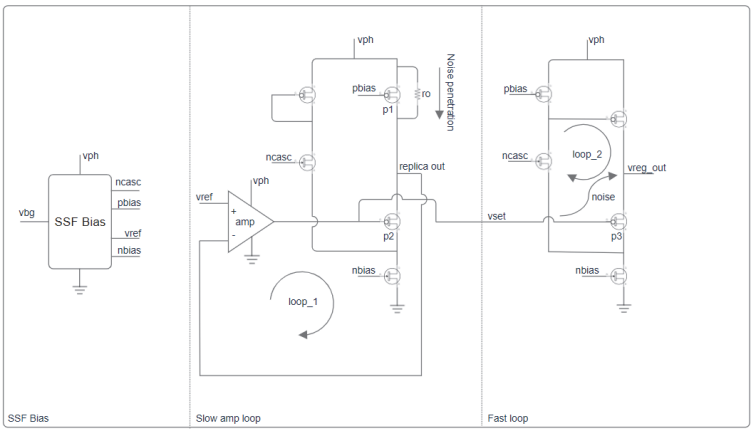

Fig. 3. SSF VREG DC PSRR deterioration problem in a standard structure

The Proposed Solution. The proposed system incorporates a digitally programmable current source circuit, an 8-bit digital controller, a high-speed comparator, and an integrated capacitor. The current source transistors, comprise eight binary-weighted parallel cascade current sources, with each branch controlled by a distinct digital bit, thereby providing a programmable current value with high accuracy and resolution (Fig. 4).

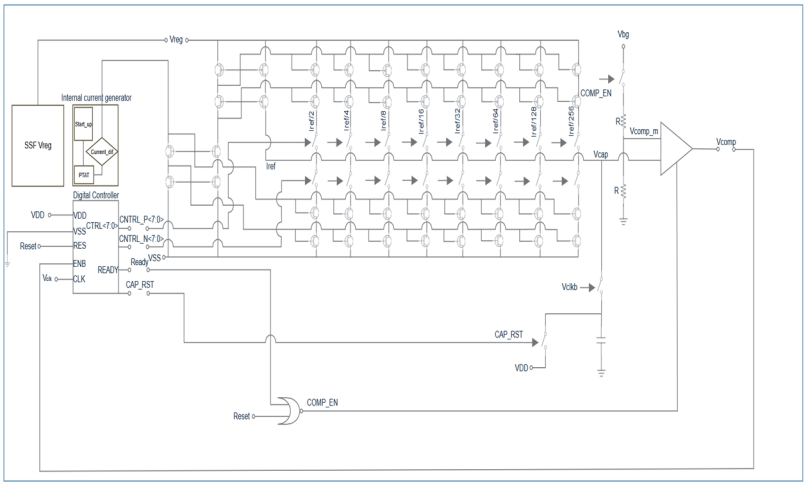

Fig. 4. The proposed current source and calibration system

The developed SSF Vreg consists of 3 loops. To ensure high speed operation of the Fast loop block, it consists of only 3 transistors. Since the Fast loop is located outside the main loop, in order to obtain an accurate output voltage, a replica cell of the fast loop was designed in the slow amp block. therefore, obtaining the intended voltage at the output of the slow amp ensures that the same voltage will be obtained at the output of the fast loop block.

$$vref = gain * xvbg \quad (1)$$

where vbg is the output voltage of the bandgap; gain - the amplifying factor of the bias block: gain = 2.25; The transistor p1 has a fairly small resistance, which is due to the small potential difference of its drain source.

$$replica\_out = vref \quad (2)$$

At the highest value of xvbg at the output of the Slow amp we obtain:

$$replica\_out = vref = 2.25 * xvbg = 0.945V \quad (3)$$

At the minimum value of the supply voltage VDD_min = 0.994 V, the potential difference of the drain source of the transistor p1 will be:

$$Vds = VDD - replica\_out = 0.994 - 2.25 * vbg = 0.994 - 0.945 = 50\ mV \quad (4)$$

Due to the small output resistance of the transistor p1, the noise penetration occurs. In the Slow amp, the operational amplifier generates an error signal *vset* to maintain a fixed output of the slow amp – the Replica Out. The *vset* is the control signal for the p3 transistor, which, in turn, is the input transistor of the source follower located in the Fast loop. The error signal generated by Loop_1 will freely pass to the vreg output - vreg_out. To prevent the noise penetration into the Slow amp, a replica of the transistor p1 located in the Slow amp (replica p1) is developed in the bias block (Fig. 5).

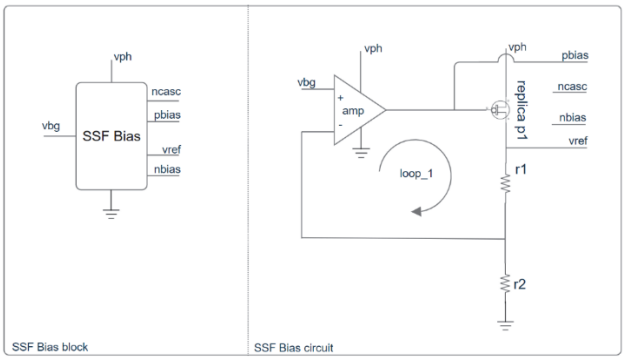

Fig. 5. A Bias block of SSF VREG

The noise penetration occurs again in the bias block for the same reason as in the Slow amp. The operational amplifier put in the bias block generates an error signal *pbias* at its output to ensure that the output of the bias block *vref* remains constant. Since this error signal is also a control signal for the transistor p1 in the Slow amp, it turns out that a noise-free signal *replica Out* will be received at the output of the Slow amp. It is necessary that for the p1 and replica p1 transistors the same operating conditions and the same dimensions are provided. The absence of noise on the Replica Out will lead to the fact that the operational amplifier putted in the Slow amp will not generate an error signal, therefore, the *vset* will be a noise-free signal. Unlike the previous case, a noise-free signal will be received at the input of the source follower, therefore, there will be a noise-free signal at the *vreg* output as well. (Fig. 6).

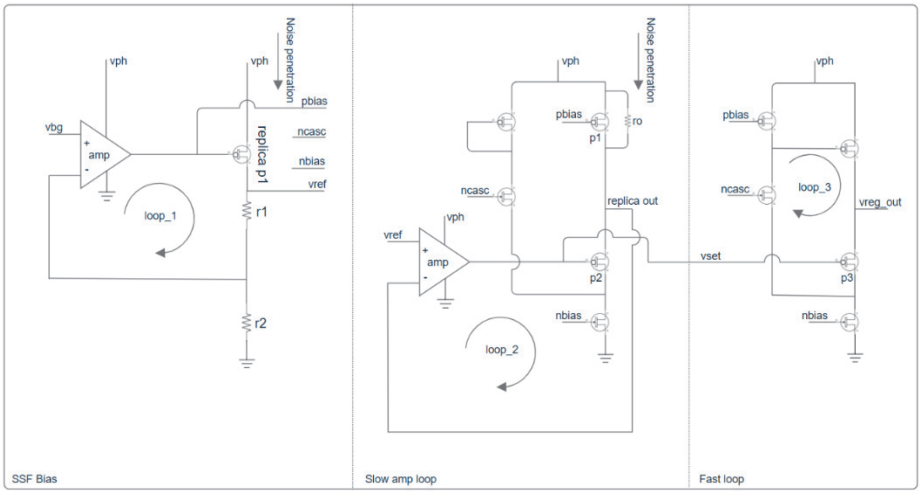

Fig. 6. SSF VREG DC PSRR improvement

When drawing up the layout of a circuit, it is necessary to take into account some nuances. First of all, it is necessary that the transistors replica p1 and p1 be located as close as possible to each other. The Fast loop block and its replica installed in Slow amp should be positioned as close to each other as possible. All the replica transistors must be perfectly matched to be in the same operating conditions.

Simulation Results. To confirm the reliability of the theoretical analyses, Spice modeling was performed using 5 nm FinFET technology. Frequency analysis was performed to check the stability of the system (Fig. 7).

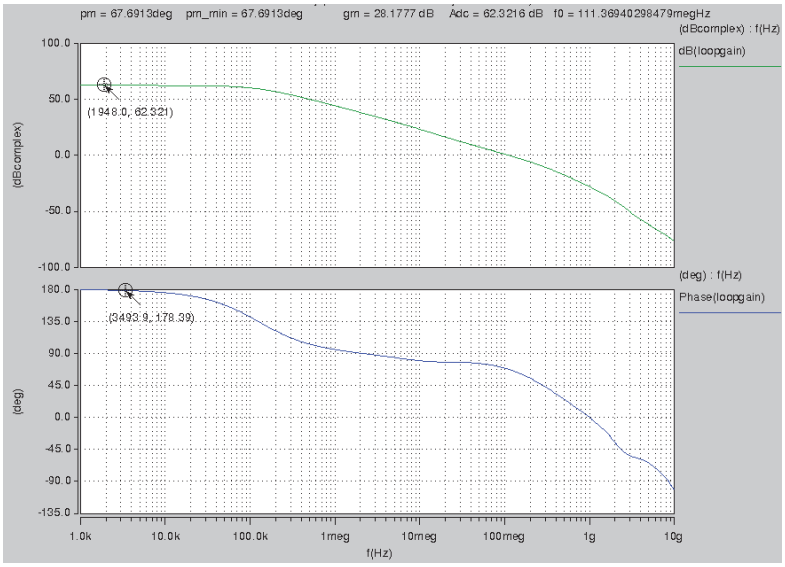

Fig. 7. SSF VREG stability for the typical case

The results obtained, depending on changes in voltage, temperature and process, show that the system is sufficiently stable (Table 1).

Table 1

Measurement	min	typ	max
adc (dB)	41.9	62.2	67.29
pm (deg)	58.36	67.78	76.77
gm (dB)	24.22	29.29	32.52
f0 (megHz)	70.9	111.26	155.07

A time analysis of the dependence of the output voltage on temperature, supply voltage and process changes was carried out (Fig. 8). From the results obtained, it can be seen that the system provides a change in the output voltage by ± 5% depending on the changes in the parameters listed above (Table 2).

Table 2

Measurement	min	typ	max
vreg_out (V)	0.82	0.84	0.85

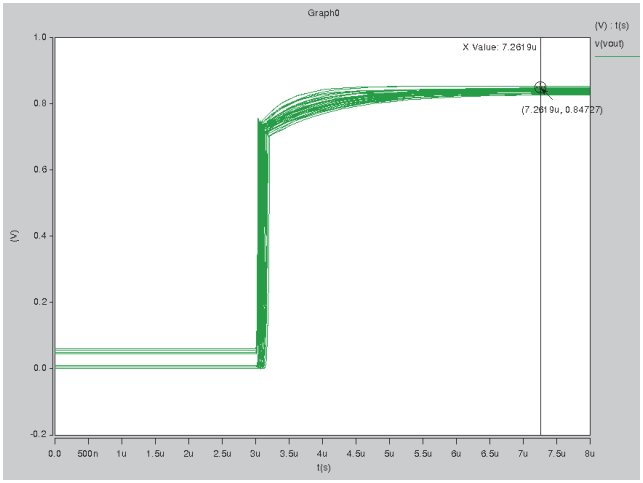

Fig. 8. The dependence of the output voltage

A frequency analysis was performed to verify the PSRR of the system (Fig. 9). From the results obtained, it is obvious that the system provides, in the worst case, -35 dB DC PSRR and -19 dB AC PSRR in the frequency range up to 10 GHz (Table 3).

Table 3

Measurement	min	typ	max
dc_psrr (dB)	-49.42	-40.84	-34.58
ac_psrr (dB)	-25.05	-22.75	-18.41

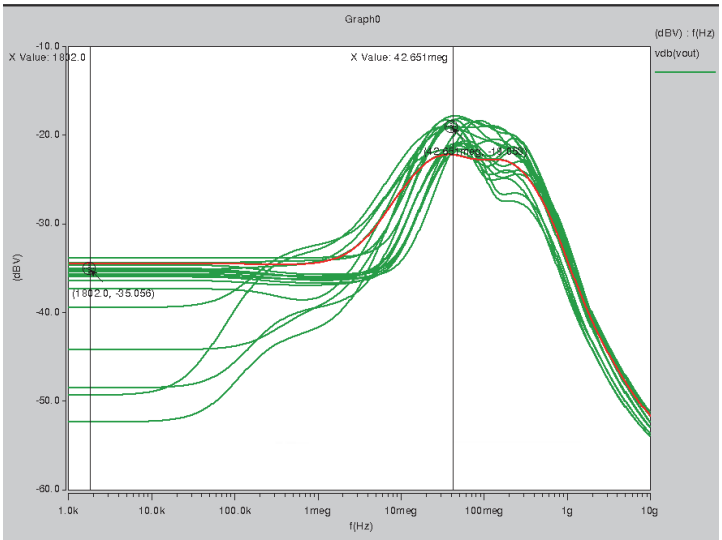

Fig. 9. The results of the frequency analysis

The simulation of the proposed circuit, utilizing a digital controller, was conducted under typical operating conditions.

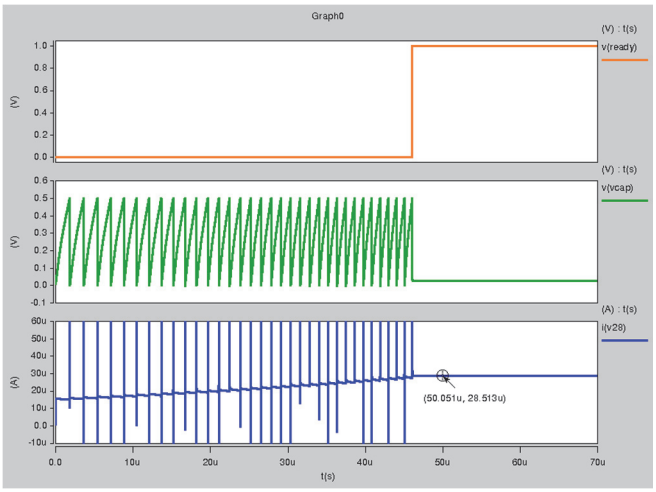

Fig. 10. The dependency of the reference current on the ambient temperature variation

In this specific scenario, it was observed that the initial current output was measured at 15 µA (Fig. 10). The results show that the reference current variation for the -40...125^{0}C temperature range considering the process variations in ±3 sigma range and supply voltage variation in ±10% range is less than 7% (Fig. 11).

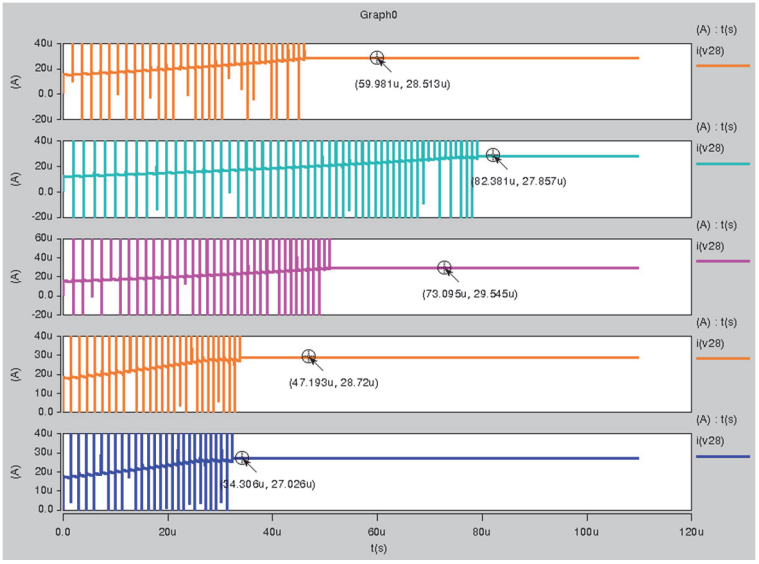

Fig. 11. The dependence of the output current on temperature, as well as supply voltage and technological changes

In summary, the results demonstrate that the variation in reference current is maintained at less than 7% throughout the specified temperature range, accounting for both process variations and fluctuations in supply voltage. This performance characteristic highlights the circuit's reliability and its appropriateness for integration into diverse electronic applications, where precise current regulation is critical for optimal operational performance.

Conclusion.

In this paper, a novel design technique for voltage regulators has been proposed, designed and simulated. According to those simulations the new circuit is capable to provide an accurate output voltage and operate in -40..125^{0}C temperature and ± 15% supply variations ranges by providing -35dB DC PSRR compared to the existing architecture, which provides lower DC PSRR values. The main limitation of the technique is the usage of a bias block as well as the estimated area increase by 10%. Both requirements are acceptable considering more relaxed requirements for such parts of IC.

REFERENCES

1. **Razavi B.** Design of Analog CMOS Integrated Circuits. - International Edition. - 2001.
2. **Yosef-Hay Yoni, Larsen Dennis Øland, Llimos Muntal Pere, Jørgensen Ivan Harald Holger.** Fully Integrated, Low Drop-Out Linear Voltage Regulator in 180 nm CMOS// Analog Integrated Circuits and Signal Processing. - 2017. - P. 427 – 436.
3. **John C.** Understanding power supply ripple rejection in linear regulators // Analog Applications Journal. - 2005. - P. 8 – 10.
4. Area-efficient linear regulator with ultra-fast load regulation **/P. Hazucha, T. Karnik, B.A. Bloechel, C. Parsons, et al //** IEEE Journal of Solid-State Circuits. - 2005. - Vol. 40. - P. 933-940.
5. A capacitor-free, fast transient response linear voltage regulator in a 180nm CMOS / **A.N. Deleuran, N. Lindbjerg, M.K. Pedersen, P.L. Muntal, et al** //Nordic Circuits and Systems Conference (NORCAS). – 2015. - P. 1-4.
6. **Manda M., Pakala S.H., Furth P.M.** A multi-loop low-dropout FVF voltage regulator with enhanced load regulation//IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS). – 2017. - P. 9-12.

Վ.Ա. ՍԱՀԱԿՅԱՆ, Ռ.Մ. ՍՈՂՈՄՈՆՅԱՆ

ԲԱՐՁՐ ՃՇՏՈՒԹՅԱՄԲ, ԼԱՐՄԱՆ ԵՎ ՋԵՐՄԱՍՏԻՃԱՆԻ ԿՈՄՊԵՆՍԱՑԻԱՅՈՎ ՀՈՍԱՆՔԻ ԱՂԲՅՈՒՐ ԹՎԱՅԻՆ ՈՒՂՂՄԱՄԲ ՏԵԽՆՈԼՈԳԻԱԿԱՆ ԳՈՐԾԸՆԹԱՑԻ ՇԵՂՈՒՄՆԵՐԻ ՀԱՄԱՐ

Առաջարկվել է նոր մեթոդիկա՝ լարման կայունարարներից սնուցվող հոսանքի աղբյուրների աշխատանքի վրա աղմուկների ազդեցության նվազեցման համար: Ելքային P – ՄՕԿ տրանզիստորով լարման կայունարարը նախագծվել է բարակ օքսիդ տրանզիստորներով ելքի 2 *մՍ* բեռի դեպքում: Մեթոդիկան արդիական է 5 *նմ* և ավելի ցածր տեխնոլոգիաների դեպքում: SPICE վերլուծության արդյունքները ցածր հաճախությունների դեպքում ցույց են տվել վատագույն -35 *դԲ* Էլեկտրաէներգիայի ճնշման հարաբերակցություն ջերմաստիճանի -40..125^{0}C փոփոխման տիրույթում, սնուցման լարման մինչև 0.994 Վ աժեքների դեպքում՝ հաշվի առնելով նաև գործընթացի փոփոխությունը ±4.5 սիգմա տիրույթում: Նախագծվել են պաշտպանական սխեմաներ՝ բարակ օքսիդ տրանզիստորների անխափան աշխատանքը տարբեր ռեժիմներում ապահովելու համար:

Առանցքային բառեր. լարման կայունարար, աղմուկ, պատճեն, հենակային լարում:

В.А. СААКЯН, Р.М. СОГОМОНЯН

ИСТОЧНИК ТОКА С ВЫСОКОЙ ТОЧНОСТЬЮ, КОМПЕНСАЦИЕЙ НАПРЯЖЕНИЯ И ТЕМПЕРАТУРЫ И С ЦИФРОВОЙ ПОСТКОРРЕКЦИЕЙ ДЛЯ ВАРИАЦИЙ ПРОЦЕССА

Предложена новая методика снижения влияния шумов питания на работу источников тока, питающихся от регуляторов. Регулятор напряжения с выходным транзистором PMOS был разработан для поддержки активной нагрузки 2 *мА*. Методика актуальна для современных узлов технологии 5 *нм* и ниже. Анализ SPICE, проведенный над разработанной схемой, показал наихудшее значение PSRR -35 *дБ* на более низких частотах в широких диапазонах температур -40..125 °C и напряжений питания до 0,994 *В* с учетом отклонения процесса в пределах ± 4,5 сигма. Также была разработана схема защиты от перенапряжения для обеспечения безопасной работы основных устройств в различных режимах работы.

***Ключевые слова*:** регулятор напряжения, шум, копия, смещающее напряжение.