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AGING IMPACT MINIMIZATION ON A TRANSMITTER JITTER

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Nowadays, technological processes actively continue to shrink the transistor's channel and Moor's law is still driving the silicon market. The transistor channel gets actively shrunk, while supply voltages do not follow that much dynamics and do not get decreased by the same per-cent. This scenario increases the aging phenomenon.

The simulations of a serial-link transmitter are implemented, considering the aging process of the MOSFET device within 10 years. The aging is simulated for the idle mode of the transmitter, while pre-driver buffers are in a static state and only the PMOS or only the NMOS transistor has gate-source and gate-substrate voltage differences, hence only one of the devices is affected by the aging process. As a result, the duty cycle of pre-driver stages is distorted, which creates an extra jitter at the transmitter's output.

In this paper, a technique is proposed to ensure the same degradation for the pre-driver PMOS and NMOS transistors during the aging process. It allows to have the same delay for transitions from logic '1' to '0' and from '0' to '1', hence the duty cycle distortion will not be created. As a result, the output jitter of the transmitter gets reduced, hence increasing the noise immunity by creating an extra margin for the noise induced jitter.

Keywords: aging, transmitter, jitter, duty cycle, frequency divider, quartz generator.

Introduction. The undesirable effects are caused by bias temperature instability (BTI) and hot carrier injection (HCI) effects. The two types of the BTI effect are available, the first one is positive BTI (PBTI) and the second one is negative BTI (NBTI). The PBTI affects the NMOS transistors while PMOS transistors suffer from the NBTI. The NBTI effect on the PMOS transistors is more dominant than the PBTI effect on the NBTI transistors. These two effects lead to an increase in the transistor's V_{th} threshold voltage.

The HCI effect is caused by the carriers in the transistor channel which are injected and trapped into the gate oxide. This effect appears with large gate-source and gate-substrate voltages. Similar to the BTI effect, the HCI also leads to an increase in the Vth voltage. From HCI, the NMOS transistors suffer more than the PMOS transistors do [1].

Different models are available for estimating the BTI and HCI effect's impact on a MOS device. Two main types of this models are charge-based and semi-

empirical models. In a charge-based model an additional capacitor is added between the inverse region and the gate oxide. The charge of that capacitor is changed within a time period and the changing amount depends on the BTI and HCI effects. The accumulated charge by BTI has a recoverable portion, while HCI does not have. The total accumulated charge during the aging process is given below (1) [2]:

$$Q_{age}(t) = Q_{HCI}(t) + Q_{BTI,str}(t) - Q_{BTI,rec}(t), \quad (1)$$

where $Q_{HCI}(t)$ is the charge amount caused by the HCI effect, $Q_{BTI,str}(t)$ is the charge amount caused by the BTI effect and the $Q_{BTI,rec}(t)$ is the recoverable portion of the accumulated charge by the BTI effect. The accumulated charge can be calculated by the transistor model, and the threshold voltage shift can be calculated as follows (2) [2]:

$$\Delta V_{th}(t) = \frac{Q_{age}(t)}{C_{age}}, \quad (2)$$

where C_{age} is the added capacitor for aging simulation. Instead of C_{age}, C_{ox} could be used.

Problem description. The increased threshold voltage will enlarge the transition delay of the transistor. While the logic gate is static, only a part of devices will suffer from aging, as the rest of them will be closed and will have zero-biased gate-source and gate-substrate voltages.

To provide the strength signal with small rise/fall times, the data before transition is buffered and provided to the driver which will transmit the data to the receiver through the channel (Fig. 1).

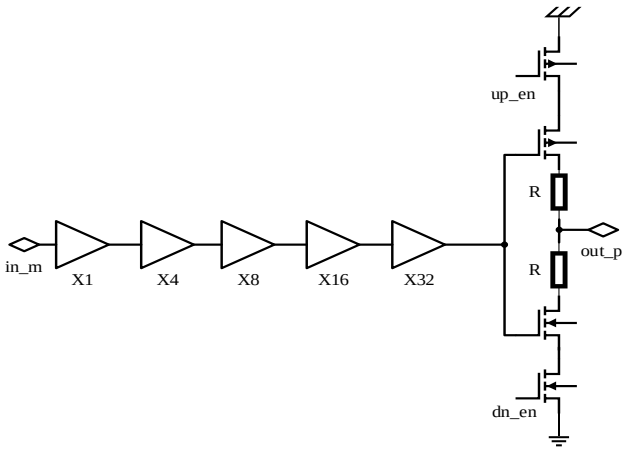

Fig. 1. Transmitter's output stage with pre-drivers

In the idle mode, there is no data to be transferred from the transmitter [3], and the inputs of the pre-driver buffers are tied to logic "1" or "0". When the buffer's input

signal is static “0”, the input PMOS device will suffer from aging and delay of switching from “0” to “1” will be increased, while switching from “1” to “0” will almost be the same as before aging. The next device which will suffer from aging in the buffer is the output NMOS device, as it has static “1” at its input, as a result, the transition delay from “1” to “0” will increase while transition from “0” to “1” will almost be the same as before aging. While the buffer input signal switches from “1” to “0”, the devices which are involved in the data transition process are the input PMOS and the output NMOS, so the delay in this case will be larger than in the case of the “0” to “1” transition. As a result, the duty cycle of the buffer will be distorted. With the number of buffers, the duty cycle distortion gets increased, as it will be accumulated through the buffer chain [4].

The aging simulations of the serial-link transmitter are implemented. The aging period is selected 10 years. While the aging transmitter was in the idle mode, after the aging impact is inserted the transmitter is simulated in the data transfer mode. The aging impact within 10 years for a 5-stage buffer chain pre-driver is presented in Fig. 2. The upper signals are the after aging results and the bottom signals are before the aging results. The plots present each buffer’s output for both cases. Before aging, the duty cycle at each buffer is almost the same. After aging, the duty cycle gets distorted and at the output of the fifth buffer, the duty cycle is 47.5%, while it is required to have a maximum +/- 1% error from 50%.

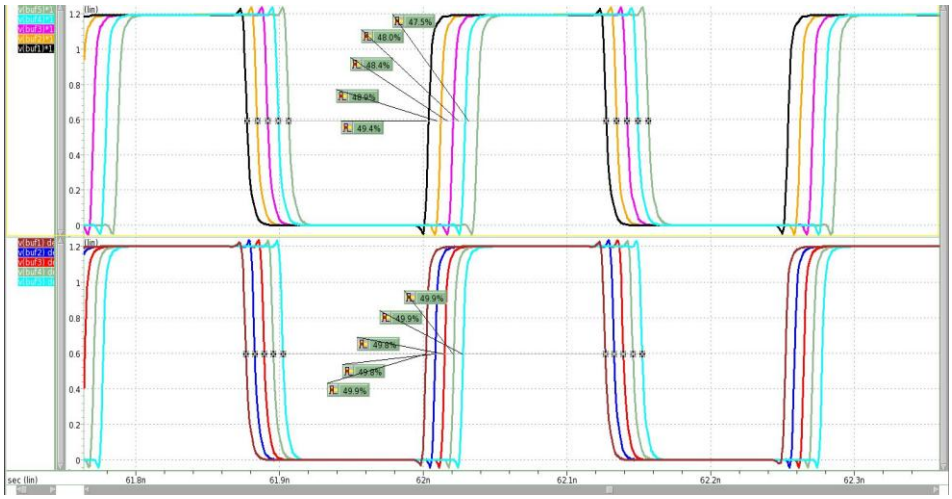

Fig. 2. The duty cycle at the buffer’s output before and after aging

The pre-driver buffers provide data to the driver stage which will transmit it to the receiver through the channel. As at the buffers output, the duty cycle is distorted, we will get the same at the transmitted data. The duty cycle distortion will create addi-

tional jitter at the output of transmitter and at the input of the receiver [5]. The transmitter's output eye diagram is presented before aging (Fig. 3) and after aging (Fig. 4).

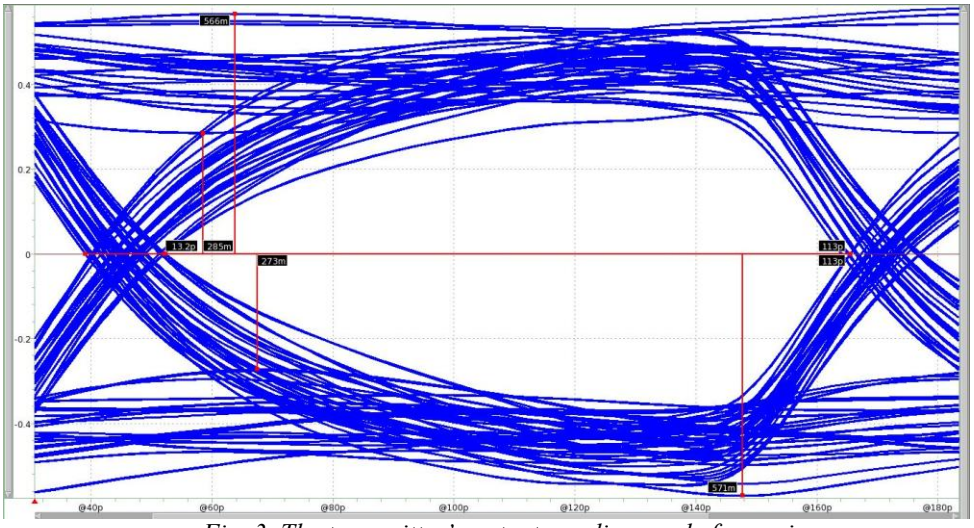

Fig. 3. The transmitter's output eye diagram before aging

Before aging the output data jitter is 13.2ps, while after aging, it is increased by 6.3ps and equals 19.5ps.

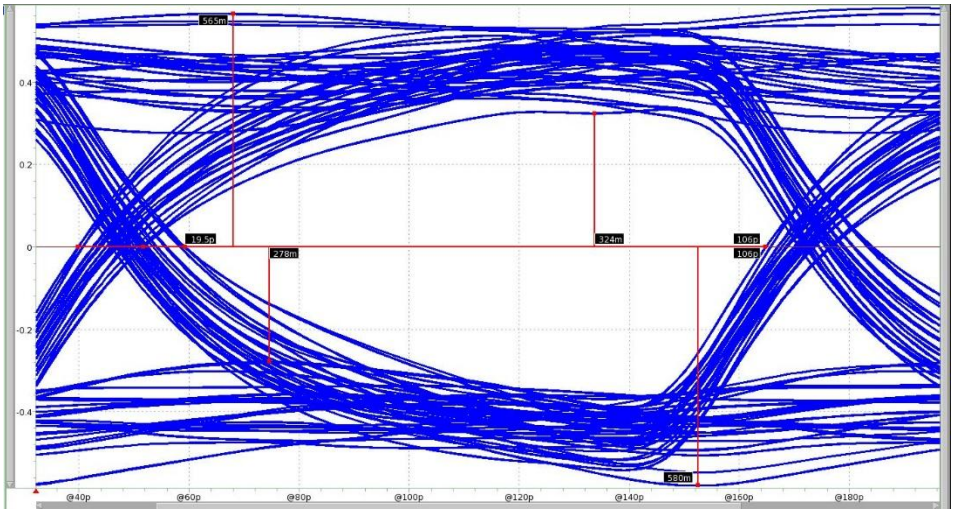

Fig. 4. The transmitter's output eye diagram after aging

The proposed solution. The technique is proposed to provide the same aging impact for all devices of the buffers to keep the symmetry of the operation. When

static “1” is applied at the buffer input, the PMOS of the input inverter and the NMOS of the output inverter will be degraded, because of gate-source and gate-substrate bias. When static “0” is applied at the buffer input, the NMOS of the input inverter and the PMOS of the output inverter will be degraded. In the case, when half of the supply is applied at the buffer input, both devices will have the same bias voltages and both devices will be degraded, but in this case, both devices will be opened and huge static current will flow through the devices.

It is proposed to change the input of the buffers during the idle mode. This will allow to degrade both the PMOS and NMOS devices of the buffers, in this way, the transition delays from “1” to “0” and from “0” to “1” will be the same and the duty cycle of the output signal will not be distorted. The output driver will be disabled by gating the “up_en” and “dn_en” signals and the output can be tied to the ground or power if it is necessary. This will eliminate the data change at the output of the driver. During the idle mode, the input is switched to a low frequency signal which is obtained from the quartz generator clock by dividing its frequency (Fig. 5).

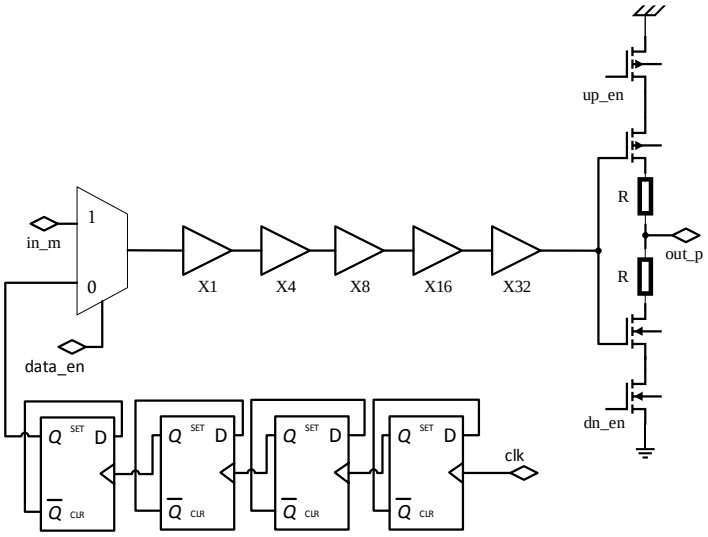

Fig. 5. A transmitter with the proposed technique

The low frequency signal provides small power consumption during the idle mode of the transmitter. The added clock dividers are built with the minimal sized transistors and will use much less power than the pre-driver buffer chain, so it is preferable to add frequency dividers to save power.

The aging simulation of the serial-link transmitter is implemented with the proposed solution with a 10 year degradation. The duty cycle for a 5-stage buffer chain pre-driver is presented in Fig. 6. The duty cycle error is 0.1%.

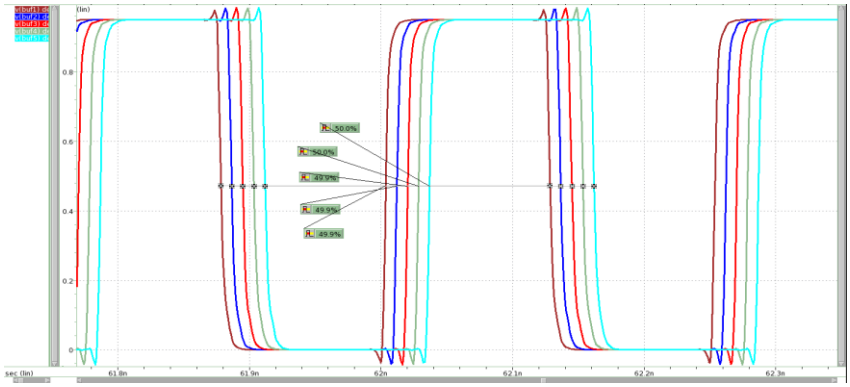

Fig. 6. The duty cycle with the proposed technique at the buffer's output after aging

The transmitter's output eye diagram after aging with the proposed technique is presented in Fig. 7. The jitter of the output signal is almost the same as before aging and equals 13.4 ps. The difference of 0.2ps is caused by rise/fall time degradation after aging.

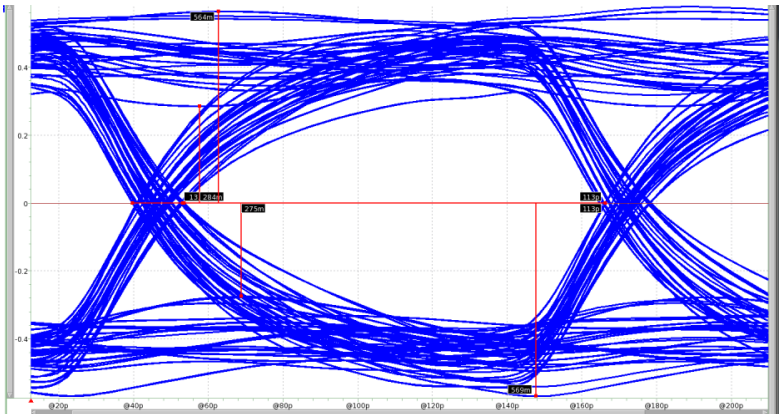

Fig. 7. The transmitter's output eye diagram after aging with the proposed technique

The summary results with the comparison of the initial and proposed methods are presented in Table.

Table

Summary results

	Initial version	Proposed technique
Duty cycle [%]	47.5	49.9
Jitter [*ps*]	19.5	13.4
Pre-driver area [um^2]	58	72
Die area [um^2]	455800	455814

***Conclusion*.** The aging simulations are implemented for a serial-link transmitter. The duty cycle distortion of the pre-driver buffer chain is observed, which is caused by asymmetrical degradation of the buffer chain. The technique is proposed to ensure the symmetrical degradation for all buffers which eliminates the degradation impact on the duty cycle of the transmitted data, hence providing the data with almost the same jitter as before degradation. The margin for a noise induced jitter, hence noise immunity is enhanced by 31% at the expense of 26% area increase of pre-driver stage and additional 32.6 uW power dissipation, which is quite small compared with transmitters 15.8 mW power consumption. Compared with total area of the transmitter-receiver system, the difference is quite small, less than 0.0001%.

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ՀԱՂՈՐԴՉՈՒՄ ԹՐԹՌՈՑՆԵՐԻ ՎՐԱ ԾԵՐԱՑՄԱՆ ԱԶԴԵՑՈՒԹՅԱՆ ՆՎԱԶԱՐԿՈՒՄԸ

Ա.Կ. Հայրապետյան

Ներկայումս տեխնոլոգիական պրոցեսում ակտիվ կերպով շարունակվում է տրանզիստորների հոսքուղիների մասշտաբավորումը, և Մուրրի օրենքը դեռևս չի կորցնում իր որոշիչ դերը: Տրանզիստորի հոսքուղին շարունակում է նվազել, մինչդեռ սնուցման լարման մակարդակը համապատասխան չափով չի նվազեցվում: Վերջինս հանգեցնում է ծերացման պրոցեսի ազդեցության մեծացմանը:

Կատարվել է հաջորդական հոսքուղով հաղորդչի մոդելավորում՝ ներառելով 10 տարվա ընթացքում ՄՕԿ տրանզիստորի ծերացումը: Ծերացումը մոդելավորվել է

հաղորդչի սպասման ռեժիմի համար, որի ընթացքում նախորդող կրկնիչները գտնվում են ստատիկ վիճակում, և միայն P-ՄՕԿ կամ միայն N-ՄՕԿ տրանզիստորի փական-ակունք ու փական-հարթակ պոտենցիալներն են տարբեր. այդ դեպքում դրանցից միայն մեկն է ենթարկվում ծերացման: Արդյունքում հաղորդչի մուտքում ազդանշանի լցման գործակիցը աղավաղվում է, որը հաղորդչի ելքում լրացուցիչ թրթռոցի առաջացման պատճառ է հանդիսանում:

Առաջարկվել է միջոց՝ P-ՄՕԿ և N-ՄՕԿ տրանզիստորների հավասարաչափ ծերացում ապահովելու համար: Այդ դեպքում ստացվում են տրամաբանական “1”-ից “0” և “0”-ից “1” փոխանջատման հավասար հապաղումներ, որի արդյունքում լցման գործակցի աղավաղում տեղի չի ունենում: Այսպիսով, հաղորդչի ելքային ազդանշանի թրթռոցը նվազում է, այդ կերպ մեծացնելով աղմուկներից առաջացող թրթռոցի պաշարը և հաղորդչի աղմկակայունությունը:

Առանցքային բառեր. ծերացում, հաղորդիչ, թրթռոց, լցման գործակից, հաճախության բաժանիչ, քվարցային գեներատոր:

УМЕНЬШЕНИЕ ВОЗДЕЙСТВИЯ СТАРЕНИЯ НА ВИБРАЦИИ В ПЕРЕДАТЧИКЕ

А.К. Айрапетян

В настоящее время в технологическом процессе активно продолжается масштабирование каналов транзисторов, а закон Мура не теряет своей актуальности. Канал транзистора продолжает уменьшаться, в то время как уровень напряжения питания не уменьшается в соответствующем размере. Последнее приводит к увеличению воздействия старения.

Произведены симуляции передатчика с последовательным каналом с учетом процесса старения МОП транзистора в течение 10-ти лет. Старение моделировано для режима ожидания передатчика, в течение которого предыдущие повторители находятся в статическом состоянии, и только у P-МОП или N-МОП транзистора есть напряжения затвор-исток и затвор-сток; в этом случае только один из них подвергается старению. В результате на входе передатчика искажается коэффициент заполнения сигнала, что становится причиной возникновения дополнительных вибраций.

Предложен метод для обеспечения равномерного старения P-МОП и N-МОП транзисторов. В результате задержки переходов от логической “1” к “0” и от “0” к “1” будут одинаковыми, следовательно, искажения коэффициента заполнения не произойдет. В результате вибрации выходного сигнала проводника уменьшаются, тем самым увеличивая запас вибраций, вызванных шумами, и, как следствие, шумоустойчивость проводника.

Ключевые слова: старение, передатчик, вибрация, коэффициент заполнения, делитель частоты, кварцевый генератор.