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# A LINEARITY IMPROVEMENT METHOD FOR A HIGH-SPEED RECEIVER

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The demand for faster and more reliable data transmission has driven the development of high-speed Serliazlier/Deserializer (SerDes) systems. These systems are used in a wide range of applications, including high-performance computers, telecommunication equipment, and data centers. However, the high speeds involved in these systems can also lead to bandwidth limitation during data transmission. To address this issue, a four-level pulse amplitude modulation (PAM4) is seriously considered, as it offers higher spectral efficiency, lower loss at the Nyquist frequency, and relaxed clock speeds compared to simple binary non-return-to-zero (NRZ) signaling. The implementation of PAM4 modulation has led to the development of various high-speed I/O standards. Considering these developments, the linearity of the system became one of the main limiting factors for its performance. Therefore, it is essential to develop methods which are aimed at addressing this limitation. A linearity improvement method of high-speed dual-mode analog receivers is presented. These receivers are characterized by their ability to operate at high frequencies and the ability to provide a high level of signal integrity, which is critical for achieving high data rates and low error rates in high-speed systems. Dual mode receivers work for both NRZ and PAM4 modulations. The key advantages of high-speed receivers such as providing a high level of signal integrity, the circuit topologies, operating modes, and performance characteristics are discussed. The usage of the proposed method improves RLM by 6% and 1$dB$ compression point by 119 $mV$ in typical corner resulting in a 7% area increase.

***Keywords:*** SerDes, transmitter, linearity, signal integrity, receiver, modulation, RLM.

***Introduction.*** Despite the fact that technological improvements have enabled enhanced high performance I/O circuits, the bandwidth of electrical channels utilized for communication between devices has not kept pace. This emphasizes the relevance of four-level pulse amplitude modulation (PAM4), which provides higher efficiency, less loss at high frequencies, and slower clock rates than regular binary communication. Current-mode, voltage-mode, and hybrid transmitters have been developed, along with both analog-to-digital converter (ADC) based [1,2] and mixed-signal receivers, to support PAM4 modulation. However, compared to NRZ-based systems, PAM4 transceivers require more stringent circuit linearity,

equalizers that can implement multi-level inter-symbol interference (ISI) cancellation, and improved sensitivity.

To achieve the high output swing required for PAM4 modulation, source-series-terminated (SST) voltage-mode drivers [3] are used on the transmitter side. These drivers provide high linearity up to differential output swings equal to the nominal output stage supply. Advanced hybrid drivers employing current boosting can further improve the output swing [4]. Voltage mode drivers also offer reduced static power consumption compared to current-mode drivers. However, at higher data rates, this advantage becomes a smaller percentage of the total transmitter power consumption due to large clocking power and the use of output-stage segmentation for equalization setting and impedance control. The presence of equalization tap-select multiplexers in the output segments can introduce on-chip ISI, including digitally controlled redundant segments for impedance control [5] results in the increased output stage area and power. Another transmitter bottleneck is the final serializer, where efforts have been made to minimize power consumption in both current-mode and voltage-mode implementations.

The receiver in high-speed serial communication systems also employs equalization to support channels with higher losses (Fig. 1).

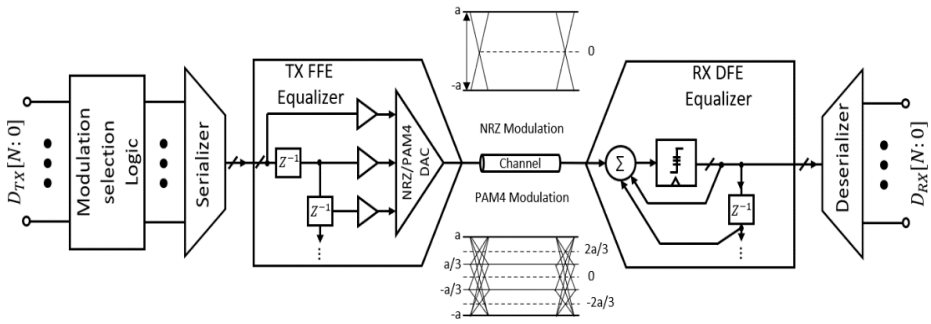


*Fig. 1. The block diagram of the high speed SerDes system*

The most common blocks for this purpose are the continuous-time linear equalizer (CTLE) and decision feedback equalizer (DFE). CTLE is useful in canceling both pre-cursor and long-tail inter-symbol interference (ISI), but CTLE amplifiers must be designed with sufficient bandwidth and linearity to support PAM4 modulation [6]. On the other hand, DFE is effective in canceling ISI without amplifying noise or crosstalk. However, optimizing the critical feedback path for ISI cancellation beginning at the first post-cursor is a significant challenge associated with DFE architectures. With PAM4 modulation, there is a longer unit interval (UI) time, but reduced voltage margins require increased comparator gain to achieve a symbol decision in one UI. In addition, DFEs using common finite impulse

response (FIR) feedback filters may require a large tap count to cancel long-tail ISI. An alternative is to use infinite impulse response (IIR) feedback filters, which can cancel exponentially decaying ISI with minimal taps, like a continuous-time equalizer. Finally, a PAM4 DFE must have the required hardware with the necessary linearity to support multi-level ISI subtraction.

Although PAM4 has advantages over NRZ signaling in terms of spectral efficiency, it is not necessarily the best modulation option for all systems. The choice of modulation depends on factors such as the desired data rate, the characteristics of the communication channel, and the process technology. In fact, most standards still use binary NRZ signaling. Since serial I/O transceivers need to support various standards and channels, it is important to have dual-mode transceivers with flexible equalization capabilities. This allows the transceiver to seamlessly support both NRZ and PAM4 modulation with minimal additional hardware and power consumption.

Linearity is an essential characteristic in high-speed SerDes receivers since the increasing data rates in modern communication systems are pushing the limits of traditional communication techniques. These high-speed signals can suffer from various distortions that affect the accuracy of the received data. Inaccurate data can lead to reduced system performance and increased error rates, which can significantly impact the system's reliability and throughput. In a SerDes receiver, linearity ensures that the receiver output signal accurately represents the input signal, even when the input signal is distorted by various impairments. A high linearity receiver can preserve the integrity of the transmitted data by maintaining a constant gain and phase response over a wide range of signal levels, allowing it to differentiate between small changes in signal level accurately. This means that the receiver can better detect and extract the transmitted signal from the noise, resulting in improved signal-to-noise ratio (SNR) and reduced bit error rates. Moreover, linearity is particularly crucial in multi-level signaling, where a single signal can represent multiple bits. In such systems, the receiver must accurately distinguish between different signal levels and correctly decode the transmitted data. This requires a high level of linearity to ensure that the receiver can accurately distinguish between different signal levels and avoid confusion between signal levels, which would lead to errors in the decoded data. For example, let's consider a 4-level signaling scheme, where each signal level represents two bits of data. In this case, the receiver must be able to distinguish between four different signal levels accurately. If the receiver has non-linearities, it may not be able to differentiate between the signal levels correctly, leading to errors in the decoded data. This can result in a reduced data rate and increased bit error rates. Therefore, maintaining linearity is essential for achieving the required performance and reliability of high-speed communication systems.

***High Speed Receiver.*** In Fig.2, a high speed receiver top level functional diagram is shown. The attenuator (ATT) includes on-die-termination, a T-coil structure that compensates for parasitic capacitances from the pad, as well as passive components for signal attenuation. It provides constant signal attenuation which should be similar to Nyquist frequency. The output of ATT is connected to continuous time linear equalizer (CTLE). CTLE provides signal equalization and conditioning, which is required for the proper operation of the slicers [7].

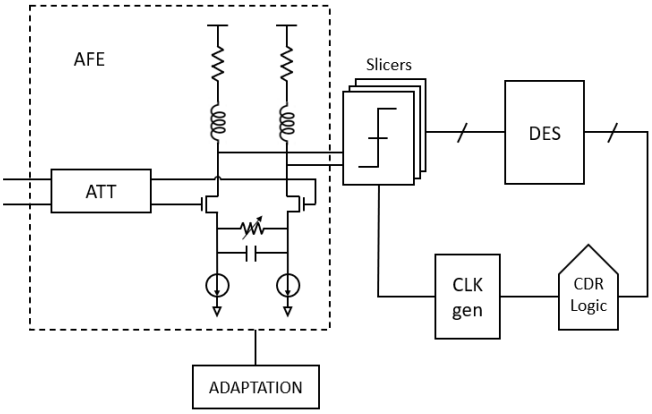


*Fig. 2. The high speed receiver top level functional diagram*

CTLE has a programmable AC gain. It has constant peaking frequency and due to programmability can have a different peak gain. Programmability is utilized by a configurable degradation resistor. By decreasing the resistance, a bigger ac gain is achieved. This option is useful in case channels with different insertion losses are used. In case of channels with lower insertion loss, a small peak gain option should be used and for bigger insertion loss cases, higher gain settings should be used. These settings are obtained after the adaptation process. The output of CTLE drive slicers which are clocked by 4 phases of the same frequency clock. In such architectures, 1 additional slicer is the part of the clock and data recovery (CDR) logic. This logic directs sampling clocks to their optimal positions.

***Problem description.*** Modern high-speed receivers are used with different channels. As an example the CEI-56G-XSR standard [8] can be taken which has a channel length up to 5 *sm*. It does not always mean that the receivers complying with this specification can only be used with 5 *sm*. Channels with shorter length have smaller insertion loss. With smaller insertion CTLE, the input amplitude is bigger which is the reason for nonlinear operation of CTLE. The main cause of non-linearity is that the input devices are getting out of the saturation region. Linearity is more critical when the receiver operates in the PAM4 mode. It will cause

relative level mismatch which has a negative impact on Bit Error Rate (BER). In Fig 3 an AFE output eye is shown with mismatch between eye openings because of the linearity limitation.

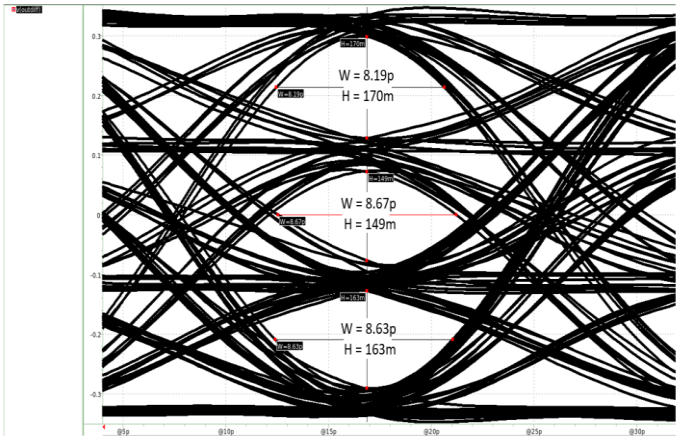


*Fig. 3. The Eye diagram with linearity limitation*

To understand the linearity of the system, we need an input and output amplitude at which 1db compression point is obtained. Before, the 1*dB* point system was considered linear. To find the 1*dB* compression point AFE input amplitude is changed from 10 *mV* to 450 *mV*. For each input amplitude point, an output signal transition is generated. After that, plots are created, with axis X representing the amplitude and the Y axis system gain (Fig. 4). By checking the plot from the starting point up to -1db location output and input amplitude values, the corresponding loss can be found. The bigger the value, the more linear the system is. Typically for modern high-speed systems, 1*dB* amplitude >500 *mV* is required. In the example shown 1db point for the input is 305 *mV* and for the output - 481 *mV*. This plot clearly shows that the system gain is varying from the input amplitude which is the main reason for non-linearity and eye-opening mismatches.

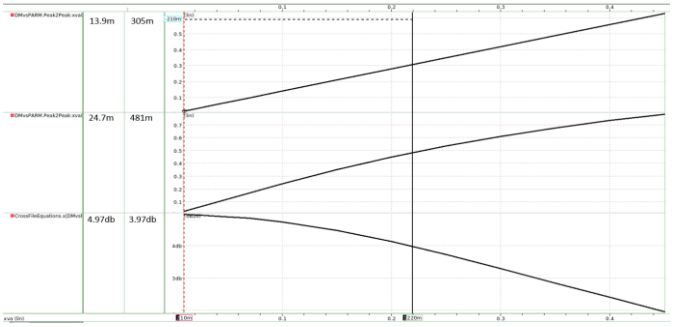


*Fig. 4. The waveform showing 1db compression point*

***The proposed method.*** To overcome the above mentioned issues, ATT with controllable attenuation is proposed (Fig. 5). An attenuator is used to reduce the amplitude of a signal without distorting it. In high-speed applications, it helps to control signal levels to avoid overloading sensitive receivers or causing data errors due to excessive voltage swings. Attenuators can be either passive or active, with the latter being more commonly used in most applications.

Regardless of frequency range, attenuators have two major paths: low-frequency and high-frequency paths. These pathways are intended to handle various frequency components of a signal while also providing proper attenuation characteristics. Low frequency path includes feedback amplifier used to set the required input common mode value for CTLE. By applying a gain control portion between positive and negative phases we can manage the attenuation value with control settings which are applied after adaptation.

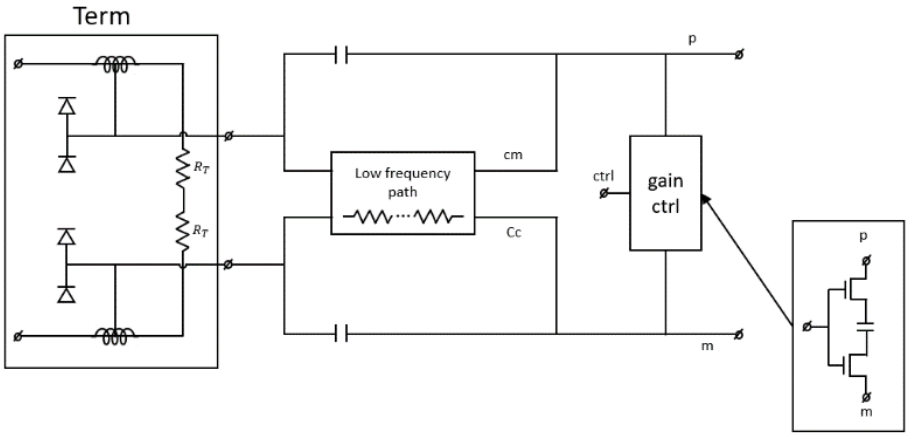


*Fig. 5. The ATT block diagram with controllable attenuation*

Gain control blocks consist of MOSFETs connected in series with a cap in between (Fig. 5). A binary coding is applied for the capacitance value control. 3 capacitors are added with increasing capacitance in a binary fashion. The first unit adds 50f capacitance, the second and third 100f and 200f, respectively. MOSFETs are used as switches and have low resistance in this implementation, hence large transistor widths are required. The biggest disadvantage of this approach is that it requires area increase. For high frequencies, ~1.5 *dB* attenuation steps with each code are achieved. The sizing decisions are made in a way to have a constant attenuation for all the AC operation range. This approach gives an opportunity to have approximately –10db attenuation (Fig. 6).

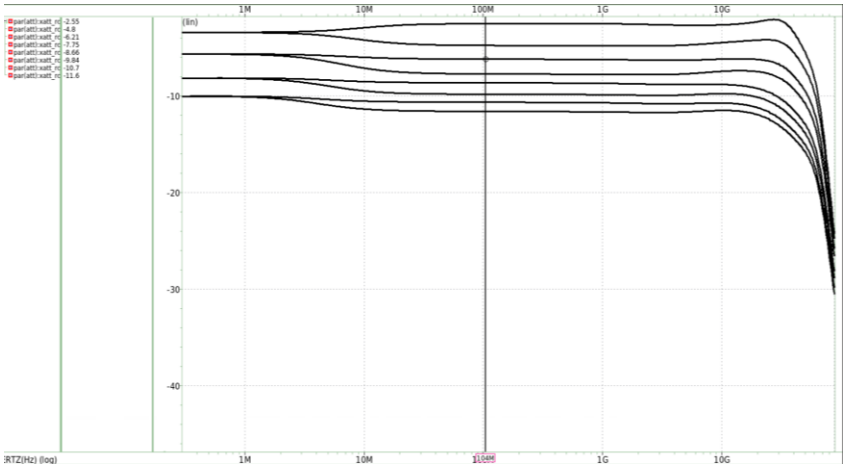


*Fig. 6. ATT frequency response across all attenuation control settings*

***Simulation Results.*** To check the proposed method's impact on the system linearity HSPICE simulation is performed using SAED 14nm technology [9,10]. In Fig. 7, the linearity of the system is shown using the same approach described in Fig. 4. It is visible that the linearity of the system improved by 119 *mV* (Fig. 7).

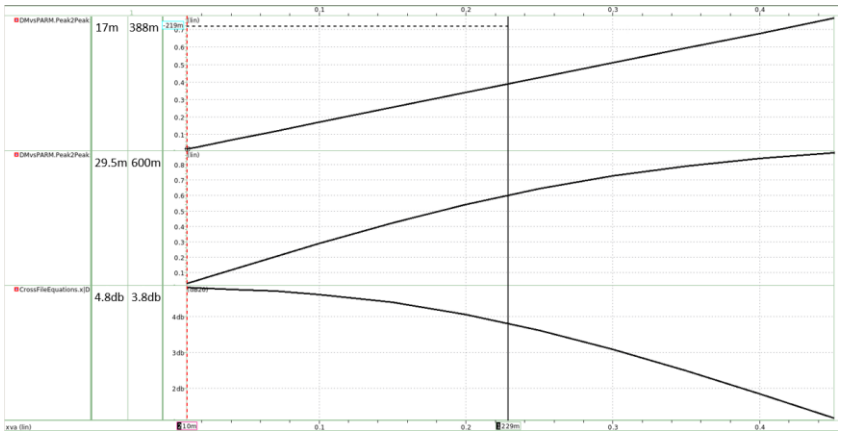


*Fig. 7. The waveform showing the improved 1db compression point*

To understand the impact of the bigger linearity, transient analysis is performed for the same corner. As seen from Fig. 8, the AFE output PAM4 eye openings are close to each other resulting in 98.6% RLM compared to 92.7% where the proposed method is not applied. Verification is performed for the SS and FF corner as well showing 140 *mV* and 108 *mV* 1 *dB* compression point improvements, respectively.

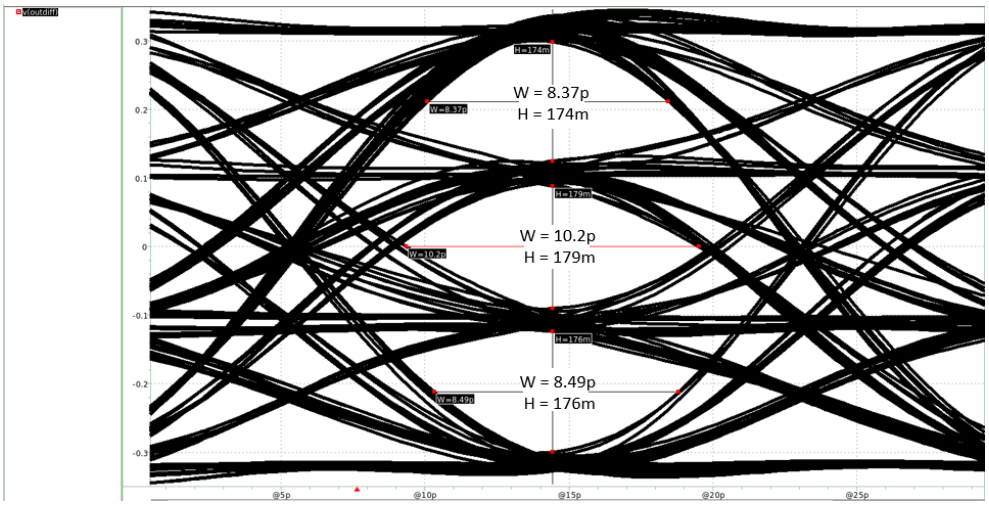


*Fig. 8. The eye diagram for thePAM4 mode*

***Conclusion.*** The analog front end with an attenuator gain control is proposed. The method improves the 1 *dB* compression point of AFE by 119 *mV*. This results in the improvement of the RLM by 6% for the typical process. Schematic updates result in 7% of the area increase from which 70% is added capacitors and the rest are MOSFET switches. The proposed method can be used in modern high speed SerDes receivers where operation with various channel lengths is supported.

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## ԱՐԱԳԱԳՈՐԾ ԸՆԴՈՒՆԻՉ ՀԱՆԳՈՒՅՑԻ ԳԾԱՅՆՈՒԹՅԱՆ ԼԱՎԱՑՄԱՆ ՄԵԹՈԴ

**Հ. Տ. Գրիգորյան, Լ. Դ. Հակոբյան**

Տվյալների ավելի արագ և հուսալի փոխանցման պահանջարկը խթանել է գերարագ Serliazlier/Deserializer (SerDes) համակարգերի զարգացումը: Այս համակարգերն ունեն կիրառության լայն շրջանակ՝ ներառյալ բարձր արդյունավետությամբ համակարգիչները, հեռահաղորդակցության սարքավորումները և տվյալների կենտրոնները: Սակայն, այս համակարգերի արագությունները կարող են հանգեցնել նաև տվյալների փոխանցման ընթացքում թողունակության սահմանափակման: Այդ խնդիրը լուծելու համար խորությամբ դիտարկվում է չորս մակարդակի ամպլիտուդի մոդուլյացիան (PAM4), քանի որ այն առաջարկում է ավելի բարձր սպեկտրային արդյունավետություն, ցածր կորուստ՝ Նայքվիստի հաճախականությամբ և տակտային ազդանշանի ցածր արագություն՝ պարզ երկուական (NRZ) ազդանշանի համեմատ: PAM4 մոդուլյացիայի իրականացումը հանգեցրել է տարբեր գերարագ մուտք/ելք ստանդարտների մշակմանը: Հաշվի առնելով այս զարգացումները՝ համակարգի գծայնությունը դարձել է դրա գործունեության հիմնական սահմանափակող գործոններից մեկը: Հետևաբար, անհրաժեշտ է մշակել մեթոդներ, որոնք ուղղված են այս սահմանափակումները հաղթահարելուն: Ներկայացված է բարձր արագությամբ երկգեժիմ անալոգային ընդունիչների գծայնության բարելավման մեթոդ: Այս ընդունիչները բնութագրվում են բարձր հաճախականություններով աշխատելու ունակությամբ և ազդանշանի ամբողջականության բարձր մակարդակի ապահովմամբ, ինչը կարևոր է մեծ արագագործությունների և հաղորդման սխալանքի փոքր արժեքի հասնելու համար: Երկռեժիմ ընդունիչներն աշխատում են ինչպես NRZ, այնպես էլ PAM4 մոդուլյացիաներով: Աշխատանքում քննարկվում են բարձր արագությամբ ընդունիչների հիմնական առավելությունները, ինչպիսիք են ազդանշանի ամբողջականության բարձր

մակարդակի ապահովումը, շղթայի տոպոլոգիաները, աշխատանքային ռեժիմները և կատարողական բնութագրերը: Առաջարկվող մեթոդի կիրառումը բարելավում է RLM-ը 6%-ով և 1 *Դբ* սեղմման կետը 119 *մՎ*-ով տիպական գործընթացում, մակերեսի 7% աճի հաշվին:

***Առանցքային բառեր.*** SERDES, հաղորդիչ հանգույց, զծայնություն, ազդանշանի ամբողջականություն, ընդունիչ հանգույց, մոդուլյացիա, RLM:

## МЕТОД ПОВЫШЕНИЯ ЛИНЕЙНОСТИ УЗЛА ВЫСОКОСКОРОСТНОГО ПРИЕМНИКА

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Потребность в более быстрой и надежной передаче данных привела к разработке высокоскоростных систем Serliazlier/Deserializer (SerDes). Эти системы используются в широком спектре приложений, включая высокопроизводительные компьютеры, телекоммуникационное оборудование и центры обработки данных. Однако высокие скорости, используемые в этих системах, также могут привести к ограничению пропускной способности во время передачи данных. Для решения этой проблемы рассматривается четырехуровневая импульсно-амплитудная модуляция (PAM4), обеспечивающая более высокую спектральную эффективность, меньшие потери на частоте Найквиста и более низкую тактовую частоту по сравнению с простым двоичным безвозвратным к нулю (NRZ) сигналом. Реализация модуляции PAM4 привела к разработке различных стандартов высокоскоростного ввода-вывода. Учитывая эти изменения, линейность системы стала одним из основных факторов, ограничивающих ее производительность. С учётом вышесказанного крайне важно разработать методы, направленные на устранение этого ограничения. Представлен метод улучшения линейности высокоскоростных двухрежимных аналоговых приемников. Эти приемники характеризуются способностью работать на высоких частотах и обеспечивать высокий уровень целостности сигнала, что имеет решающее значение для достижения высоких скоростей передачи данных и низкого уровня ошибок в высокоскоростных системах. Двухрежимные приемники работают как с модуляцией NRZ, так и с PAM4. Обсуждаются ключевые преимущества высокоскоростных приемников, такие как обеспечение высокого уровня целостности сигнала, топологии схемы, режимы работы и рабочие характеристики. Использование предложенного метода улучшает RLM на 6% и точку сжатия 1 *дБ* на 119 *мВ* в типичном процессе, что приводит к увеличению площади на 7%.

***Ключевые слова:*** SERDES, узел передатчика, линейность, целостность сигнала, приёмный узел, модуляция, RLM.