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THE OUTPUT NOISE REDUCTION OF THE MULTIPLEXER

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A new approach to reducing output noises of the multiplexer (MUX) is presented. In contrast to other methods, this one reduces the noise with a strength equal to the strength of the noise in specific cases. The method is based on adding logic cells and transistors in the circuit and choosing its sizes corresponding to the delay time of the output signal and to the strength of the output noise. In general, the main device that is used for reducing output noises in digital and analog circuits it's capacitor. But in the circuits which scheme structure depends from its bit number, the output noise strength depends from the quantity of the switching inputs of the scheme. As high will be the switching inputs, as bigger will be the strength of the output noises. The same capacitor can keep the accuracy of the output signal in certain cases of switching inputs combinations. Here is developed a method, by which each combination of switching inputs turns on appropriate output elements by which the accuracy of the output signal is saved in any case. The method is very comfortable using in MUX, because its inputs mostly are symmetrical, and it helps to use the method adding the output elements with nearly same sizes. The symmetrical structure of the inputs of the MUX is useful for the method, also observing the input-output signal delay time. By using this method on 2-to-1 MUX designed in 32 *nm* technology, the area of the circuit increases by 28% and the noise error decreases by 59%.

Keywords: MUX, XNOR, invertor, NAND.

Introduction. A multiplexer is a device that selects between several analog or digital input signals and forwards the selected input to a single output line. A multiplexer makes it possible for several input signals to share one device or resource, for example, one analog-to-digital converter or one communication transmission medium, instead of having one device per input signal. The working principle of MUX is shown in Fig.1.

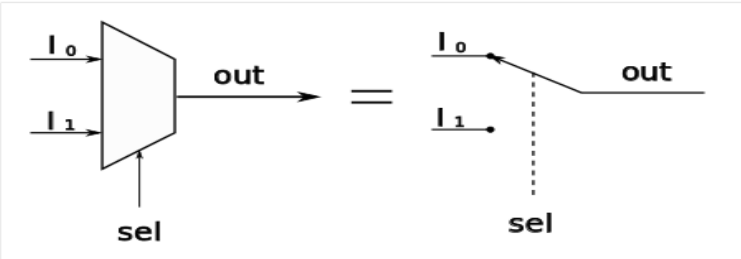

Fig.1. The scheme of a 2-to-1 multiplexer

Generally, the selection of each input line in a multiplexer is controlled by an additional set of inputs called *control lines*. Normally, a multiplexer has an even number of 2n data input lines and a number of "control" inputs that correspond to the number of data inputs.

Literature review. There are many different methods and approaches for reducing noises in the output of MUX. There are also many researches about noise impact in MUX, or impact of the noise on other circuits from MUX. For example in [1] the multiplexing error and noise reduction are described. Multiplexers introduce errors, which we have estimated by consecutive phantom measurements both using voltage multiplexers and by selecting the electrodes by hand, all other things being the same. Noise is taken care of by averaging. The difference image obtained is considered an estimation of the multiplexer induced error.

In [2], the details of the basic multiplexer work is shown.

In [3], analog signal rejection on the multiplexer is presented.

In [4], noise reduction on the multiplexing system is presented. The signal to the noise ratio of the received signal through Avalanche Photo diode in the receiver is calculated. This work identifies the best pulse generator with reduced noise performance suitable for the proposed system. The proposed system is modeled in optisys and insightful discussions are provided from the simulated results.

In [5], the frequency-domain multiple readout of transition-edge sensor arrays is presented.

In [6], analog Switches and multiplexers Basics are introduced. Switches and multiplexers of the late 1960s were designed with discrete MOSFET devices and

were manufactured in small PC boards or modules. A dielectrically-isolated family of these parts introduced in 1976 allowed input overvoltages of ± 25 V (beyond the supply rails) and was insensitive to latch-up.

In [7], some description of noise reduction and isolation is presented. Controlling noise in a measurement systems is vital because it can become a serious problem even in the best instruments and data acquisition hardware.

In [8], the invention related to optical networking and more particularly to systems and methods for Wavelength Division Multiplexing (WDM) communications is presented. Many of the current agile architectures suffer from poor optical performance, e.g., high insertion loss on added/dropped wavelengths and/or injection of additional noise on the added wavelengths. The existing fixed OADM structures are costly and perform effectively only for low counts of channels to be added or dropped and only where traffic reconfiguration or future growth is not an issue.

In [9], low frequency noise reduction technique for linear analog CMOS ICs is described. The mathematical descriptions for the noise behavior and the signal transfer of the proposed operational amplifier architecture are derived. With the help of the derived equations, the distinct features of the principle are identified

from the measurements and simulations: the noise aliasing due to the principle and the increase in the white noise plateau which attributes to thermal resistive noise increase of the switches with increasing clock frequency. Finally, it is noted that the clock mismatch parameter tp should be optimized for the best electrical performance.

This priority of the new method against the others is the reducing of the output noise keeping the accuracy of the output signal and the increase of area with not high percent.

The proposed MUX. The simplest MUX is the 2-to-1 MUX. The method is applied in 2-to-1 MUX which does not have very big noises in the output, but needs their reduction. The noise reduction 2-to-1 MUX with the new method proves that the method will be very useful for higher node MUXs. The primary circuit of 2-to-1 MUX is shown in Fig.2.

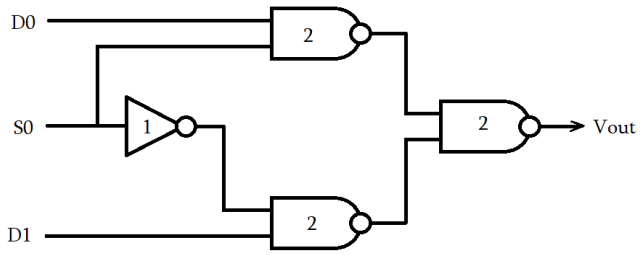

Fig.2. The primary circuit of MUX (1 - Invertor, 2 - NAND)

In general, to reduce the noises, it is preferable to use capacitors in the output of the circuit. But the strength of noise depends on the quantity of switching inputs at the same time. The more inputs are switching at the same time, the higher will be the noise in the output. If we use a capacitor which is able to reduce the output noises in case of all input switches, in case of only one input switch the capacitor, except reducing the noise, can lay down the output signal, which will not be an accurate result. So, it is necessary to use a specific structure of a circuit, which will reduce the output noises with a strength equal to the strength of the output noise. The working principle of the 2-to-1 MUX is shown in Table 1.

For example, in case of 000 to 111, or 011 to 100 the input combination changes, the noise reduction system must work corresponding to the strength of three input changes. In case of 100 to 101, the system must reduce the noise corresponding to one input change. So, instead of capacitors, a nmos transistor for the output node is used. The quantity of the output transistor is equal to the quantity of inputs. The gate of the transistor is connected to one of the inputs. In case of any input switch, the corresponding transistor turns on with a very little time range. The cells between one MUX input and its corresponding output transistors have a delay time equal to the delay time of the input-output signal transmission of the MUX, so, the transistor turns on at the same time in which the output signal of the MUX

changes causing the noises. When the output signal changes from low to high voltage, the little-time switch of the transistor makes a hole for the noise, and the noise in the output becomes much less.

Table 1

The working principle of the 2-to-1 MUX

S0	D0	D1	Vout
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

When the output signal changes from high to low voltage, the transistor switch, which also opens a road for the output voltage to 0, does not leave the output signal to oscillate around 0 voltage. So, in this case, output noises become much less, too. The cell which connects the input node to the output transistor is shown in Fig.3.

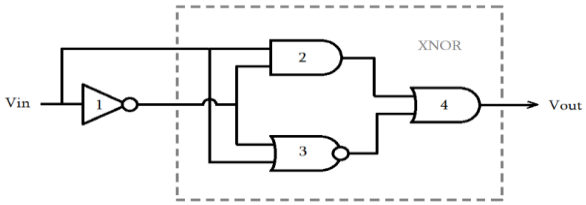

Fig.3. The cell connecting the input node to the output transistor in MUX (1 – Invertor, 2 – AND, 3 – NOR, 4 - OR)

The working principle of XNOR is shown in Table 2.

Table 2

The working principle of XNOR

In1	In2	Out
0	0	1
0	1	0
1	0	0
1	1	1

The output-input dependency of the cell connecting the input node on the output transistor in the MUX is shown in Fig.4.

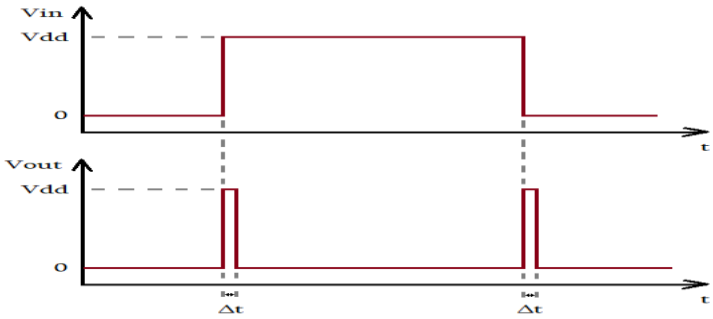

Fig.4. The output-input dependency of the cell connecting the input node on the output transistor in MUX (Vin – input signal, Vout – output signal, Vdd – supply voltage, Δt – very little time range)

So, the noise impact of each input switch on the output signal will be neutralized by the corresponding output transistor, and in case of any quantity of switching inputs, the output noises will be reduced by appropriate strength, which is conditioned by a quantity of switching output transistors, and the output signal will be accurate in any case of the input combination change. The Δt time range is conditioned by the switch time of the invertor. The optimized MUX is shown in Fig.5.

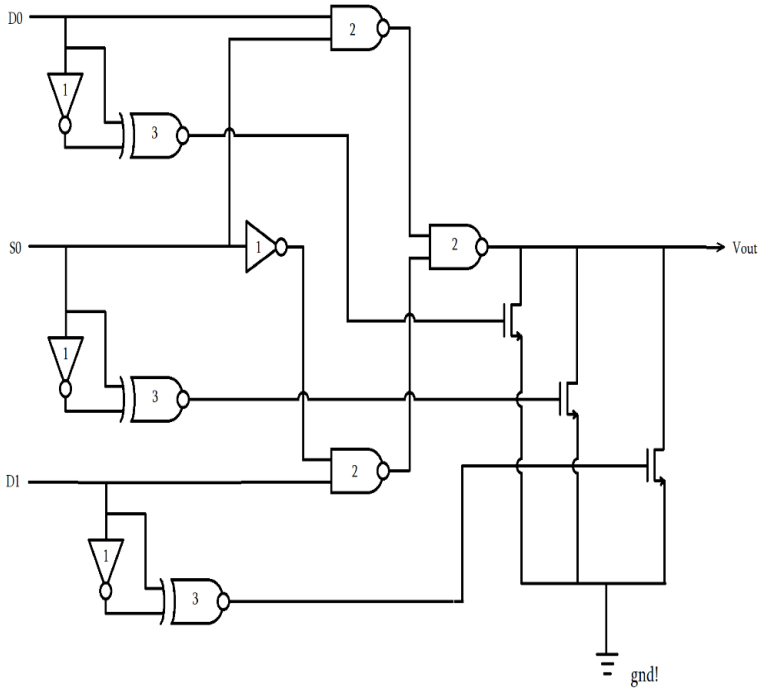

Fig.5. The optimized MUX (1 - Invertor, 2 - NAND, 3 - XNOR)

This method can be applied to other circuits too, but for MUX it is very comfortable, because the general inputs of the MUX are symmetrical, and the impact of each input node on the output signal is proportional to the other inputs. That makes the usage of the method more simple, as the output transistors and cell connecting the input node to the output transistor in MUX can be designed in the same way for each MUX input (appropriate to the MUX input-output delay, and to the strength of the output noises). The only disadvantage of the method is that the area becomes a bit higher.

Simulation results. The main block of the MUX is designed. Simulations are performed using the HSPICE simulator (described in [10]) for a number of PVT corners including 3 main conditions (TT, FF and SS processes with respective voltage and temperature values). Here the results of the TT typical corner are presented. The circuit is designed and simulation is performed in the 32 *nm* technology. The simulation results of the primary 2-to-1 MUX are shown in Fig.6 with input and output characteristics. Supply voltage is 2.5 *V*. S0 is the choosing input. DO and D1 are the inputs that must be chosen. This MUX is designed for maximum 4 *GHz* frequency and has got 0.01*W* power consumption.

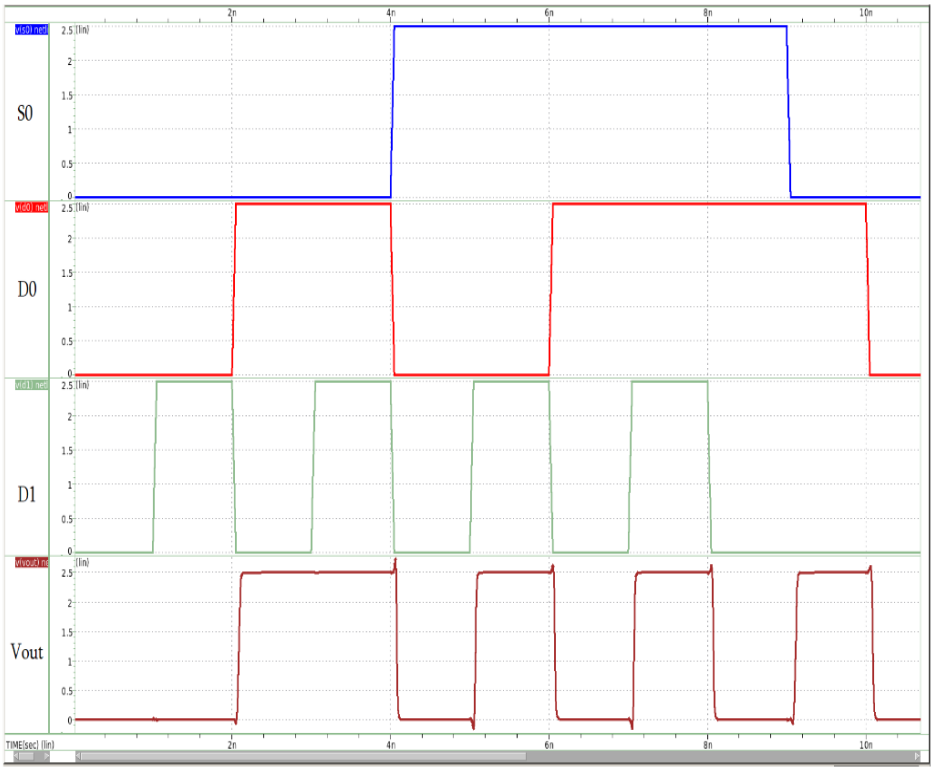

Fig.6. The simulation results of the primary MUX designed in 32 nm technology

The highest noise is on the first fall time of the output signal. The output voltage changes from 2.5 *V* to 2.72 *V*.

In Fig.7 the simulation results of the optimized MUX are shown.

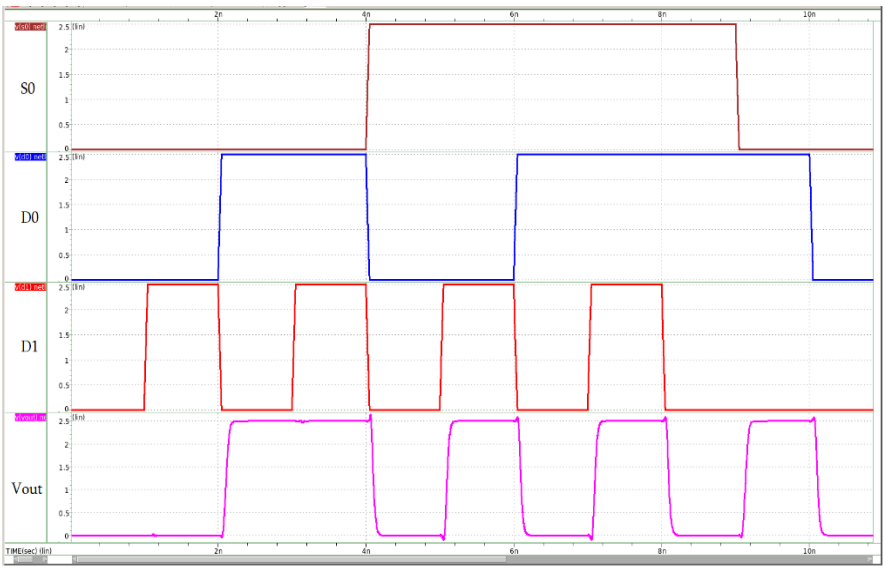

Fig.7. The simulation results of the optimized MUX designed in 32 nm technology

The highest noise is on the first fall time of the output signal. The output voltage changes from 2.5*V* to 2.63*V*.

The circuit of the primary 2-to-1 MUX circuit designed in the 32 *nm* technology is shown in Fig.8.

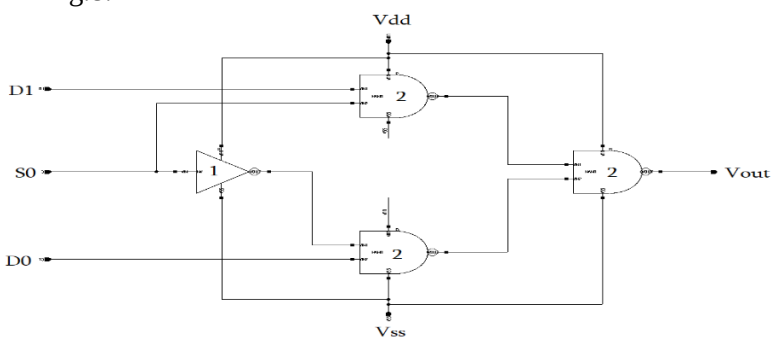

Fig.8. The primary 2-to-1 MUX designed in 32 nm technology (1 - Invertor, 2 - NAND)

The circuit of the optimized 2-to-1 MUX circuit designed in the 32 *nm* technology is shown in Fig.9.

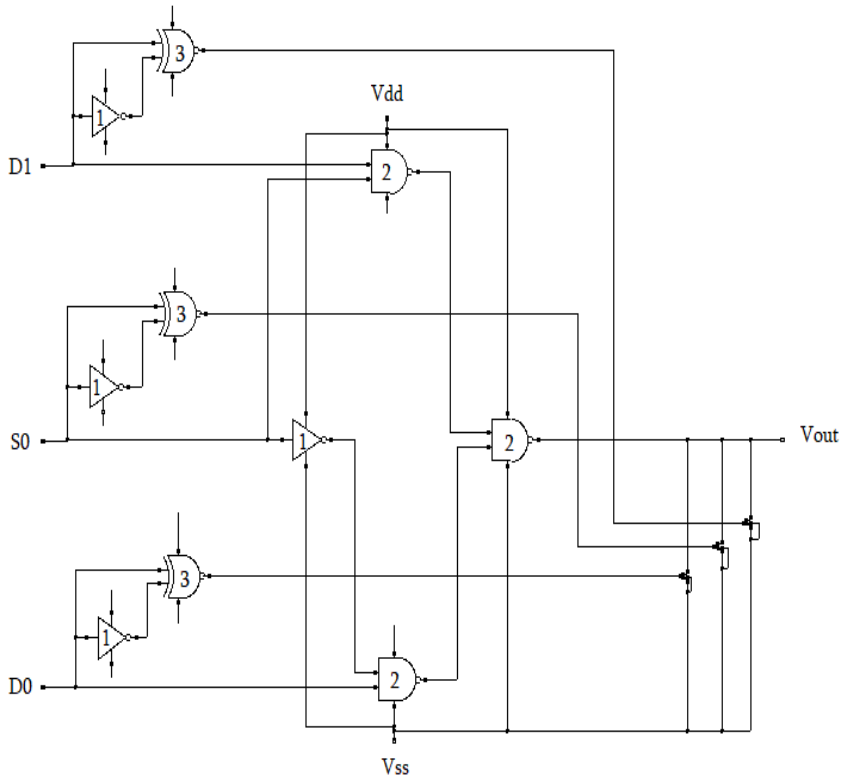

Fig.9. The optimized 2-to-1 MUX designed in 32nm technology (1 - Invertor, 2 - NAND, 3 - XNOR)

The area of the circuit is increased by 28% at using the method.

Conclusion. A new method for noise reduction of the MUX is presented. The main advantage of this method is that it reduces noise with a strength equal to the strength of the noise in any case of the input combination change. This new method requires an increase of the area by a low percent. It can be less in case of MUX with higher quantity of inputs and outputs. In the 2-to-1 MUX designed in 32 *nm* technology, area is increased with 28% by using the method, but output noises becomes less with minimum 59%. The method is also preferable to use in the circuits different than MUX, but for MUX it is very preferable, as it has got symmetry in its inputs, which makes the design of the additional circuit part much easier. It means that it is preferable to use the method for MUX with a very large circuit in difference with other schemes whose circuit becomes complicated in case of the large number of inputs and outputs.

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ԵԼՔԱՅԻՆ ԱՂՄՈՒԿՆԵՐԻ ՆՎԱԶԱՐԿՈՒՄԸ ՄՈՒԼՏԻՊԼԵՔՍՈՐՈՒՄ

Հ.Ա. Բաբաջանյան, Ս.Խ. Խուդավերդյան

Ներկայացված է մուլտիպլեքսորի ելքային աղմուկների նվազեցման նոր մոտեցում: Ի տարբերություն այլ մեթոդների՝ այս մեթոդը նվազեցնում է աղմուկը նրա ուժգնությանը հավասար ուժով որոշակի դեպքերում: Մեթոդը հիմնված է միացման մեջ տրամաբանական բջիջների և տրանզիստորների ավելացման և դրա չափերի ընտրության վրա, որոնք պետք է համապատասխանեն ելքային ազդանշանի հետաձգման ժամանակին և ելքային աղմուկի ուժգնությանը: Ընդհանուր առմամբ, հիմնական տարրը, որն օգտագործվում է թվային և անալոգային սխեմաներում ելքային աղմուկները նվազեցնելու համար, կոնդենսատորն է: Բայց այն սխեմաներում, որոնց շղթայական կառուցվածքը կախված է իրենց սխեմայի բիթայնությունից, ելքային աղմուկի ուժգնությունը պայմանավորված է սխեմայի փոխանջատվող մուտքերի քանակով: Որքան բարձր կլինեն փոխանջատվող մուտքերը, այնքան ավելի մեծ կլինի ելքային աղմուկների ուժգնությունը: Միևնույն կոնդենսատորը կարող է պահպանել ելքային ազդանշանի ճշգրտությունը փոխանջատվող մուտքերի կոմբինացիաների որոշված դեպքերում: Մշակվել է մեթոդ,

որով փոխանջատվող մուտքերի յուրաքանչյուր համակցություն ստեղծում է համապատասխան ելքային տարրերի կառուցվածք, և ըստ որի ճշգրիտ ելքային ազդանշանը պահպանված է ցանկացած դեպքում: Մեթոդը շատ հարմար է օգտագործել մուլտիպլեքսորում, քանի որ նրա մուտքերը հիմնականում սիմետրիկ են, և այդ փաստը թույլ է տալիս մեթոդն օգտագործել՝ ավելացնելով գրեթե նույն չափերով ելքային տարրեր: Մուլտիպլեքսորի մուտքերի սիմետրիկ կառուցվածքը օգտակար է մեթոդի դեպքում՝ դիտարկելով նաև ազդանշանի մուտքից ելք ժամանակային հետաձգումը: Օգտագործելով այս մեթոդը 2-ից 1 մուլտիպլեքսորի վրա, որը նախագծված է 32 նանոմետր տեխնոլոգիայով, շղթայի մակերեսը մեծանում է 28%-ով, իսկ աղմուկի սխալանքը նվազում է 59%-ով:

Առանցքային բառեր. մուլտիպլեքսոր, բացառիկ ԿԱՄ-ՈՉ, ինվերտոր, ԵՎ-ՈՉ:

МИНИМИЗАЦИЯ ВЫХОДНЫХ ШУМОВ МУЛЬТИПЛЕКСОРА

А.А. Бабаджанян, С.Х. Худавердян

Представлен новый подход к снижению выходных шумов мультиплексора. В отличие от других методов, данный метод уменьшает шум с силой, равной силе шума в конкретных случаях. Метод основан на добавлении в схему логических ячеек, транзисторов и на выборе их размеров в соответствии со временем задержки выходного сигнала и силой выходного шума. В целом основным устройством, используемым для уменьшения выходных шумов в цифровых и аналоговых схемах, является конденсатор. Но в схемах, где структура зависит от ее разрядности, мощность выходного шума будет зависеть от количества переключающихся входов схемы. Чем выше переключающиеся входы, тем больше будет сила выходных шумов. Этот конденсатор может сохранить точность выходного сигнала в некоторых случаях переключений входных комбинаций. Разработан метод, согласно которому каждая комбинация переключающихся входов включает соответствующий выходной элемент, благодаря чему точность выходного сигнала в любом случае сохраняется. Этот метод очень удобен для использования в мультиплексоре, поскольку его входы в основном симметричны, что позволяет использовать метод, добавляя выходные элементы с почти одинаковыми размерами. Для метода полезна симметричная структура входов мультиплексора, принимая во внимание также время задержки сигнала от входа до выхода. При использовании этого метода на мультиплексоре 2-1, разработанном по 32-нанометровой технологии, площадь схемы увеличивается на 28%, а шумовая ошибка уменьшается на 59%.

Ключевые слова: мультиплексор, эксклюзивное НЕ-ИЛИ, инвертор, НЕ-И.